

Tang/TangBTO Schematics Document
uFCBGA/uFCPGA Coppermine-T or Tualatin

2001-11-16

REV: 2.0

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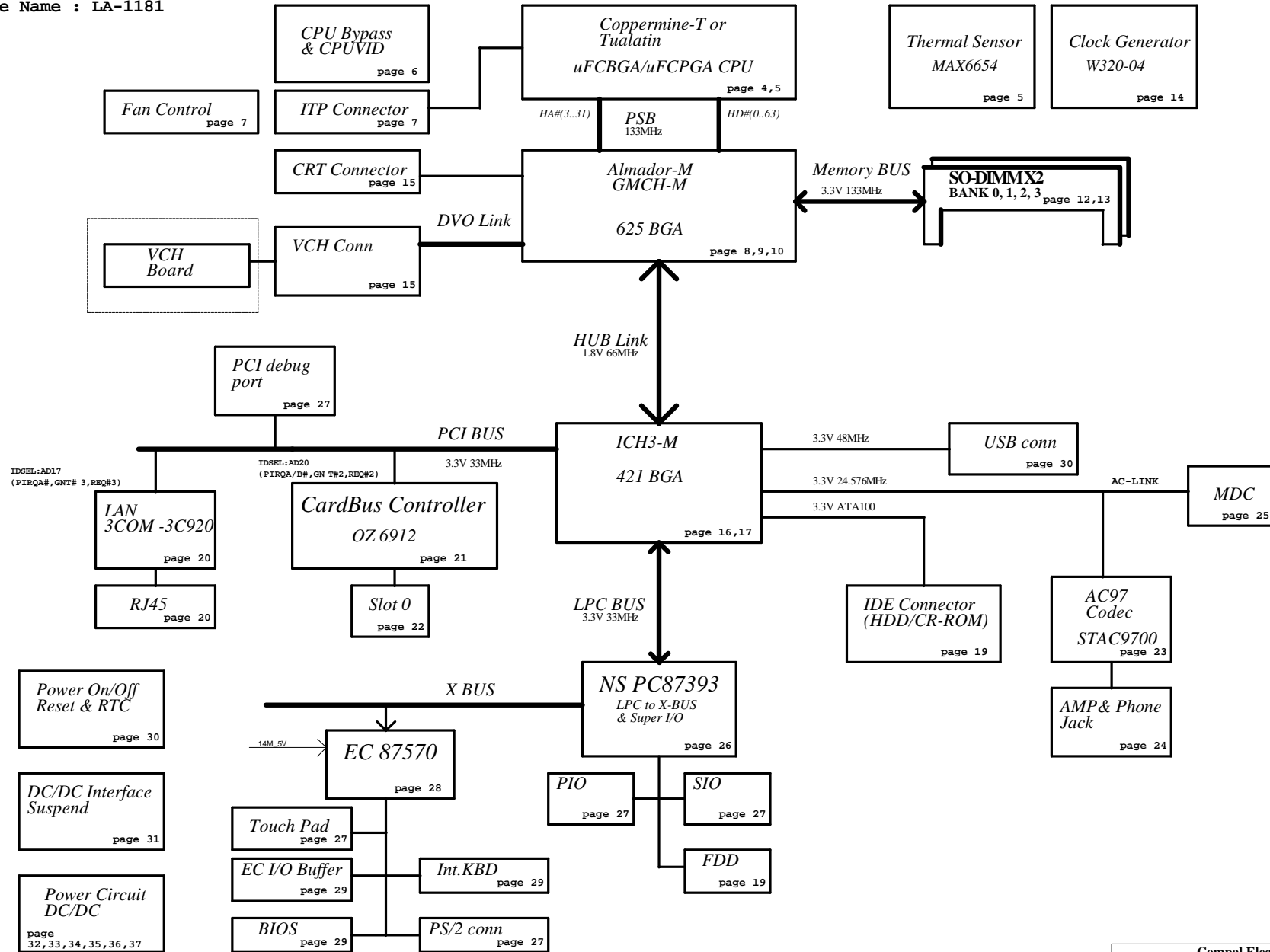
Compal Electronics, Inc.			
Title			
Cover Sheet			
Size	Document Number		Rev
	ADY11 LA-1181		2
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Compal confidential

Model Name :ADY11(Tang)

File Name : LA-1181

Block Diagram



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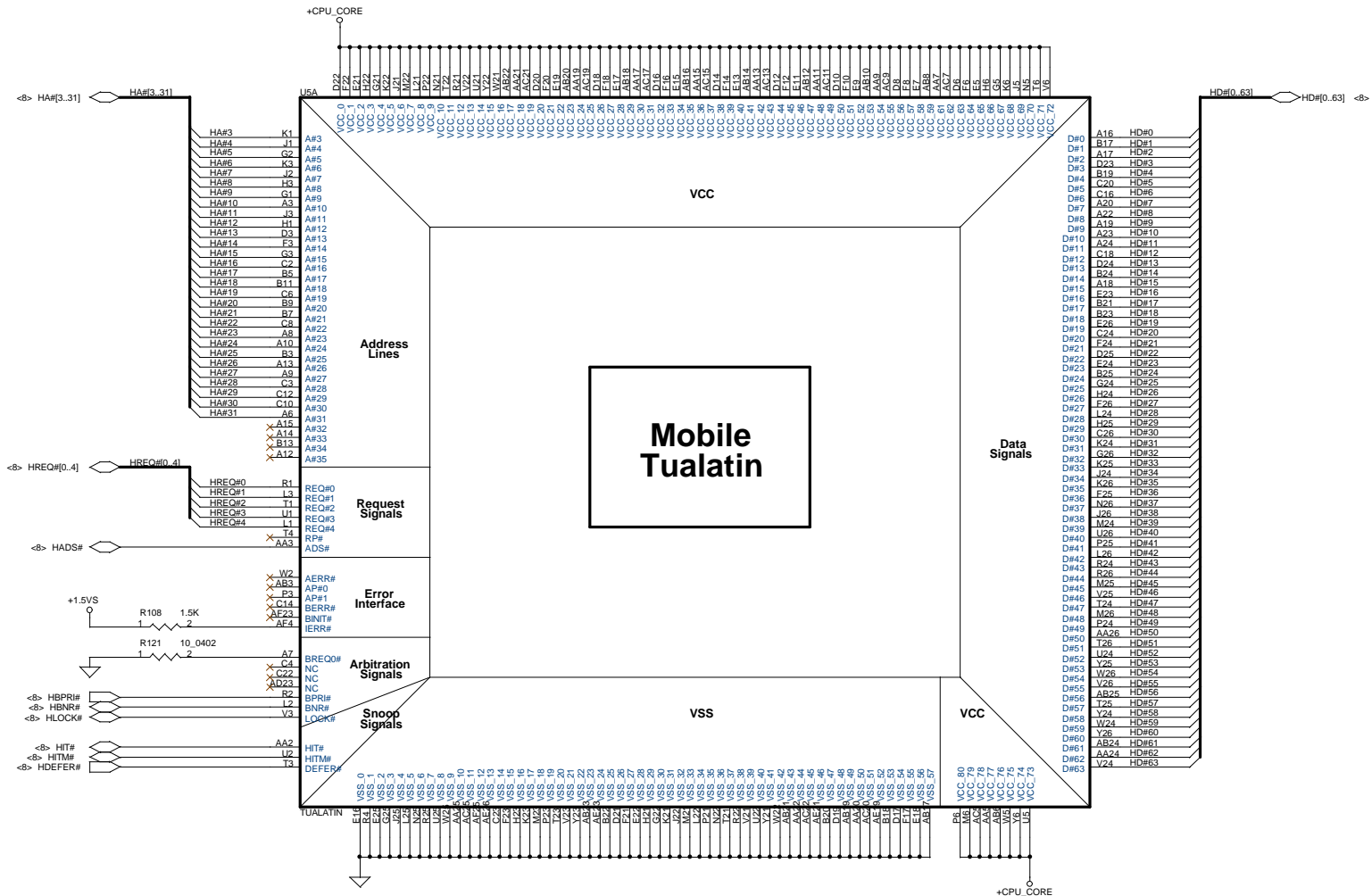
Compal Electronics, Inc.			
Block Diagram			
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Note:"@" means all model depop
"##" means Tang depop

Model Function	M2P3	Tang
FDD	YES	NO
PS/2	YES	YES
Series port	NO	NO
Parallel port	YES	YES
RJ45	YES	NO
3Com Lan chipset(3C920)	YES	NO

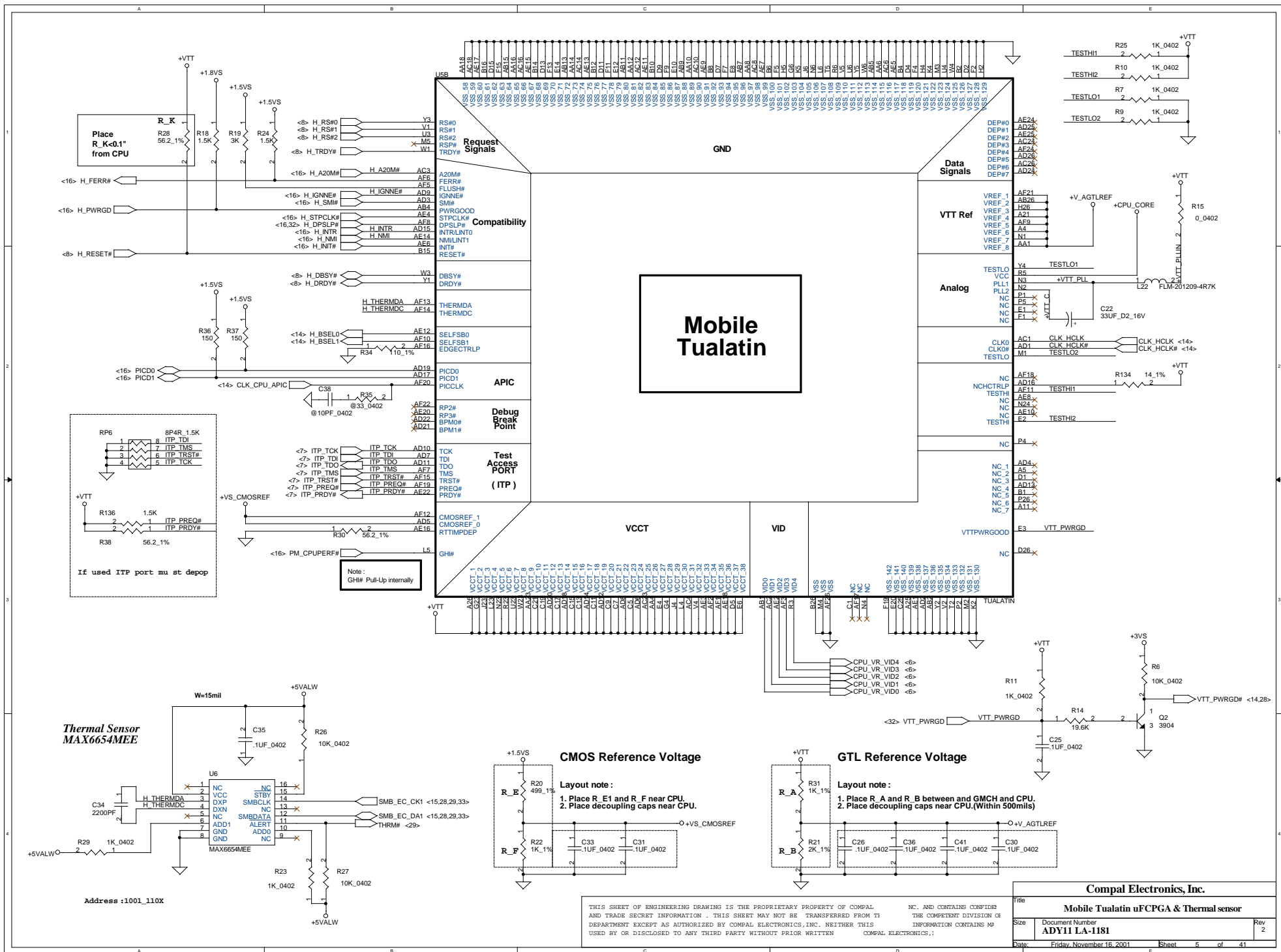
Note:"@" means all model depop
"&" means M2P3 depop
"##" means Tang depop

	CHIPS Rev	CHIPS Rev	3C920-ST06
SST-Build	FW82830MG QB88	FW82801CAM QB63	Lot:M28010 DC:C0117
SST2-Build	QC34	QB62	Lot:M28010 DC:C0117
PT-Build	QC34	QB62	Lot:M28010 DC:C0117
ST-Build	QC34	QC42	Lot:M28010 DC:C0117



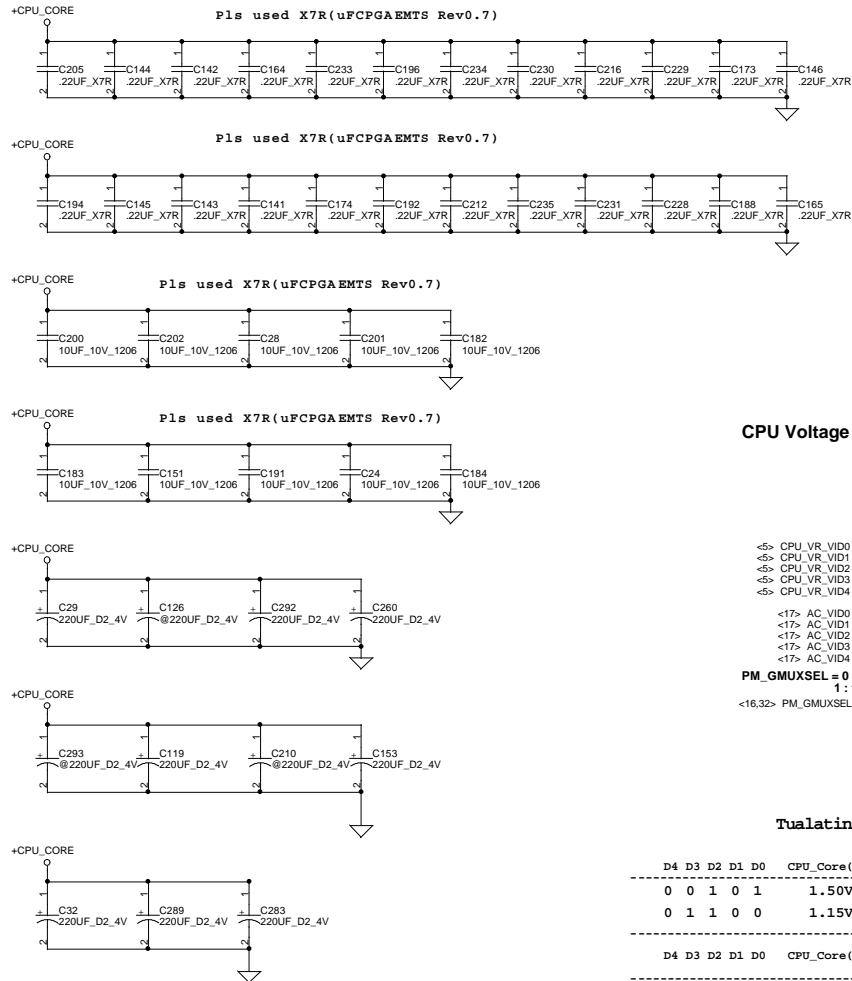
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Mobile Tualatin uFCPGA			
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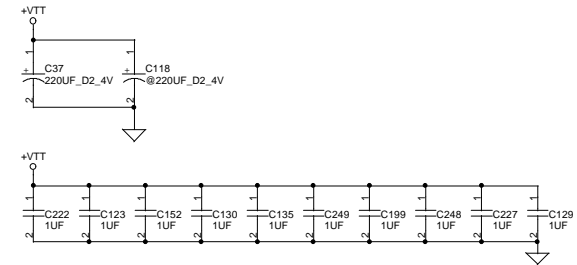
Layout note :

Place close to CPU, Use 2-3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

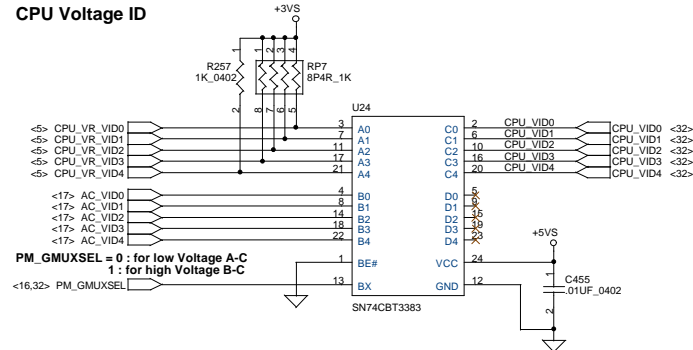


Layout note :

Place close to CPU,
Use 2 vias per PAD.



CPU Voltage ID



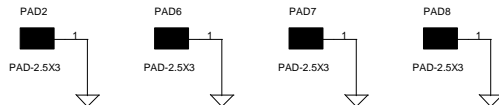
Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	ES(before	MP)
0	0	1	0	1	1.50V		
0	1	1	0	0	1.15V		
D4	D3	D2	D1	D0	CPU_Core(V)	QS	(MP)
0	0	1	1	1	1.40V		
0	1	1	0	0	1.15V		

Coppermine-T

D4	D3	D2	D1	D0	CPU_Core(V)	ES(before	MP)
0	0	0	0	1	1.70V		
0	1	0	0	0	1.35V		
D4	D3	D2	D1	D0	CPU_Core(V)	QS	(MP)
0	0	0	0	1	1.70V		
0	1	0	0	0	1.35V		

EMI Clip PAD for CPU



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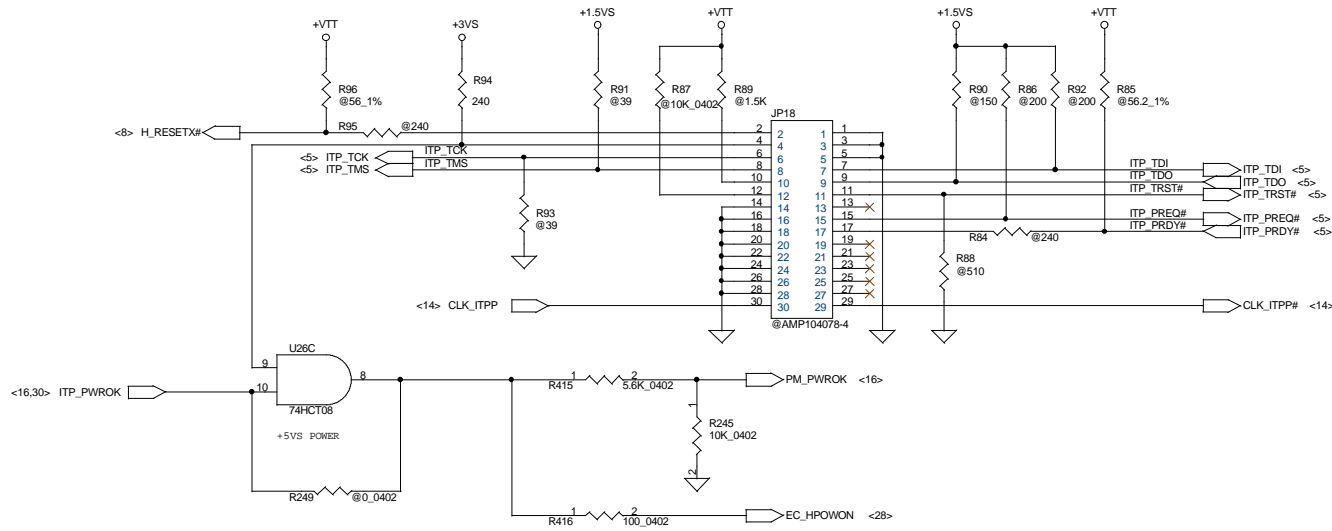
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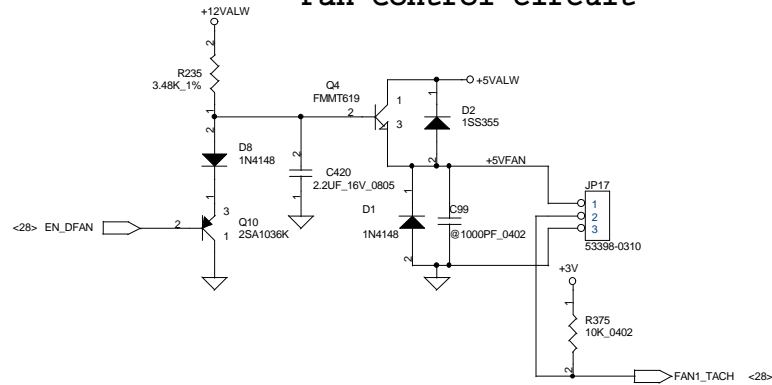
CPU Bypass & CPU VID

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ITP PORT



Fan Control circuit

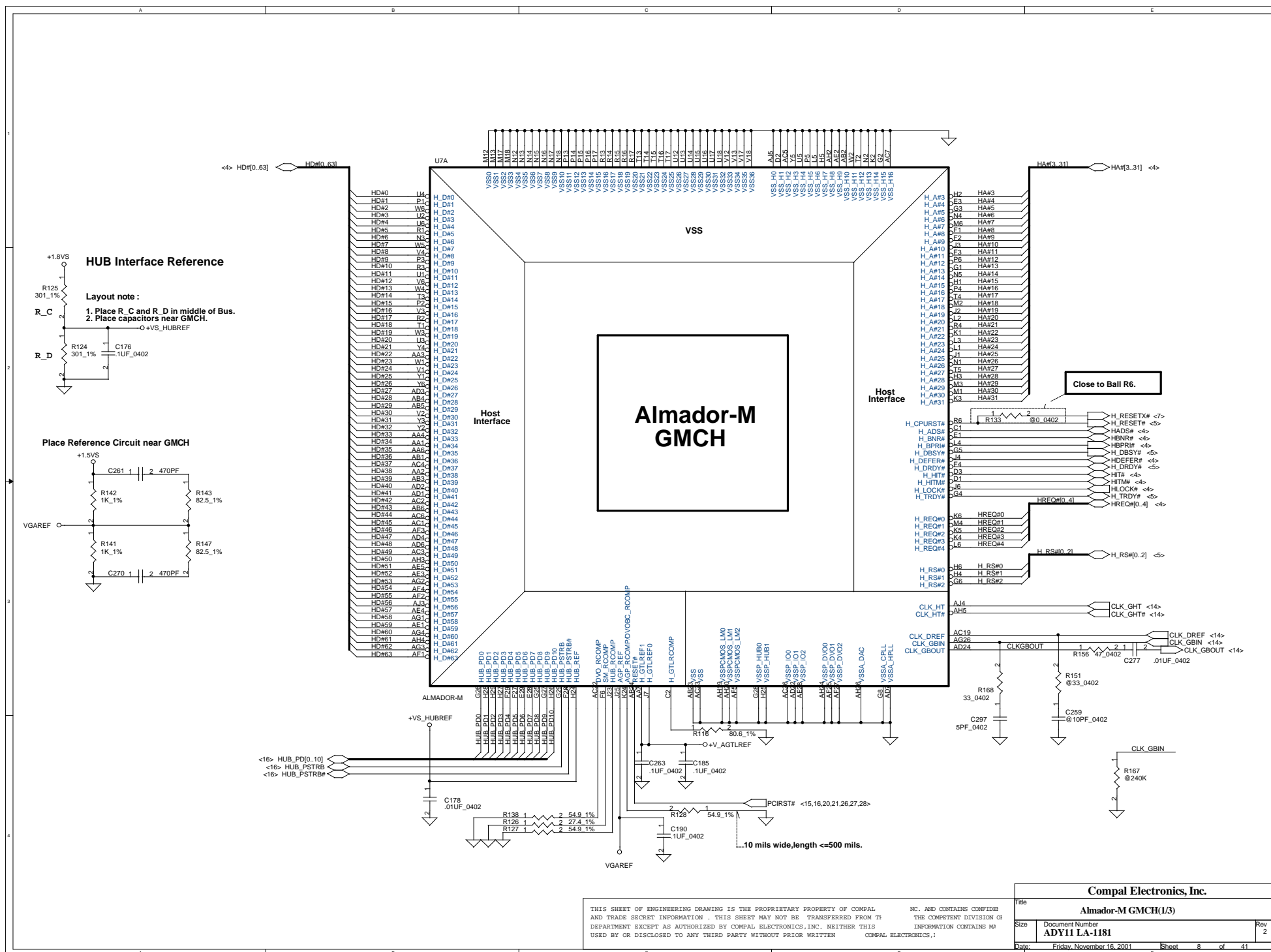


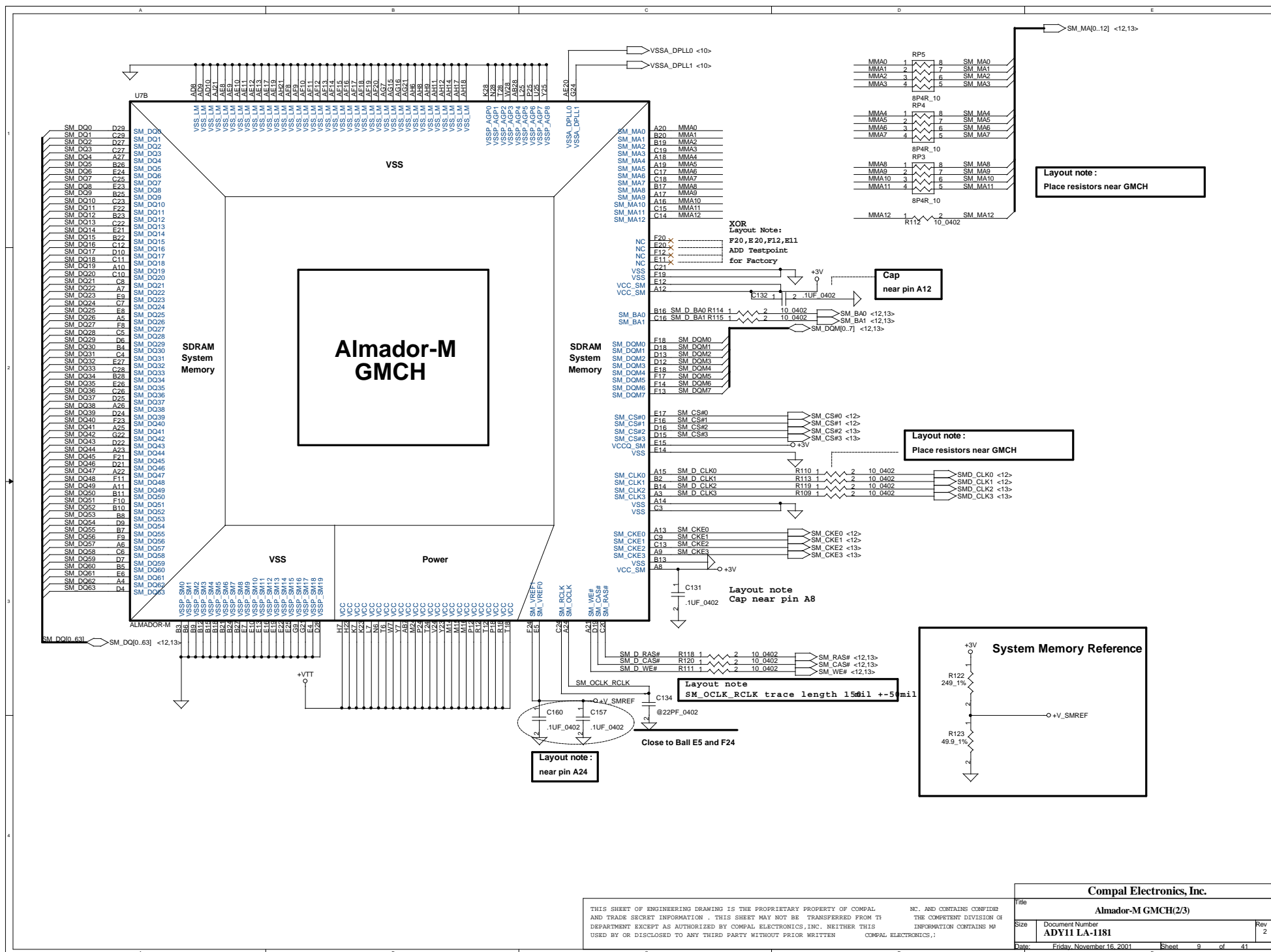
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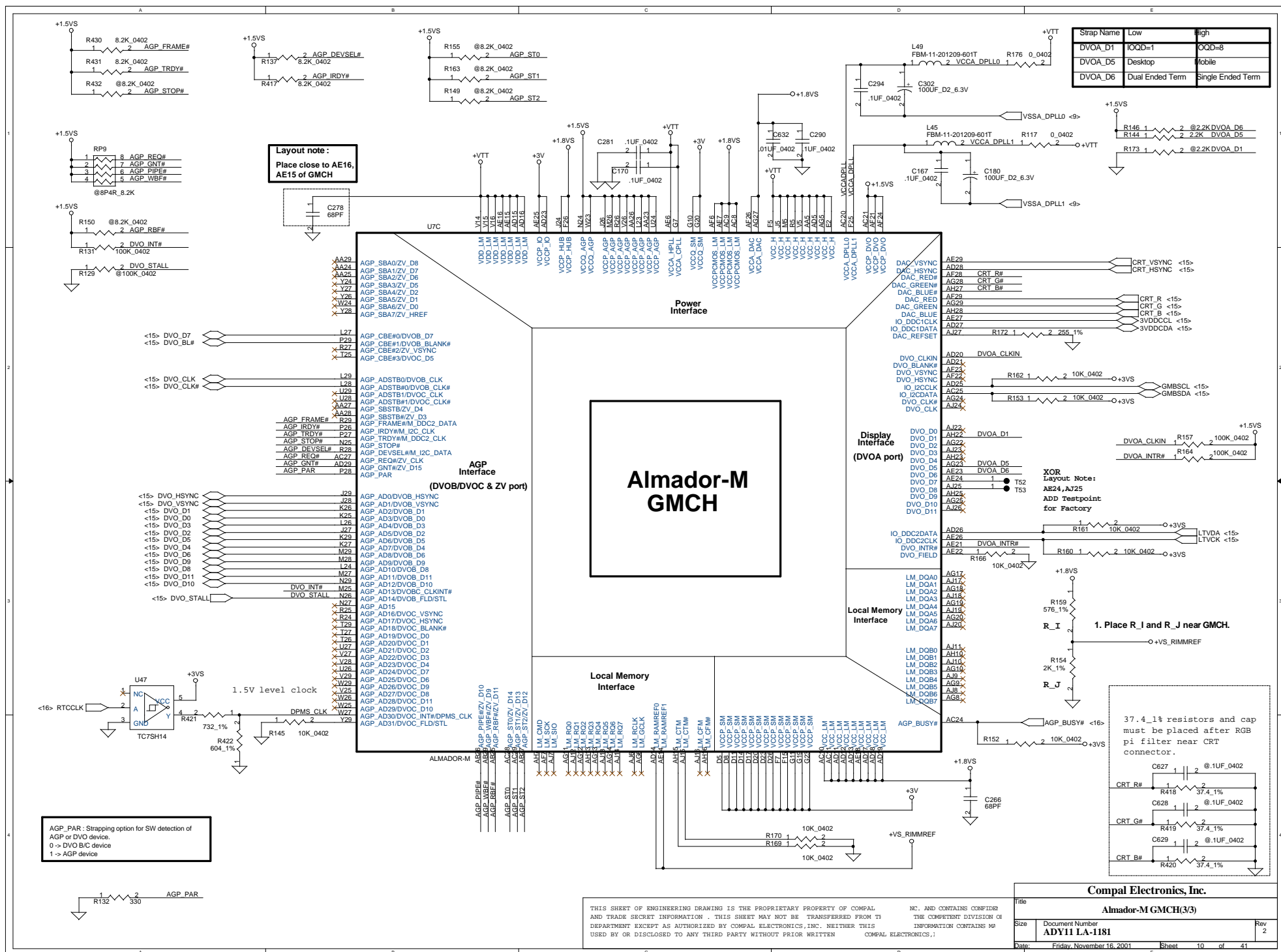
COMPAL Electronics, Inc

ITP PORT & Fan control

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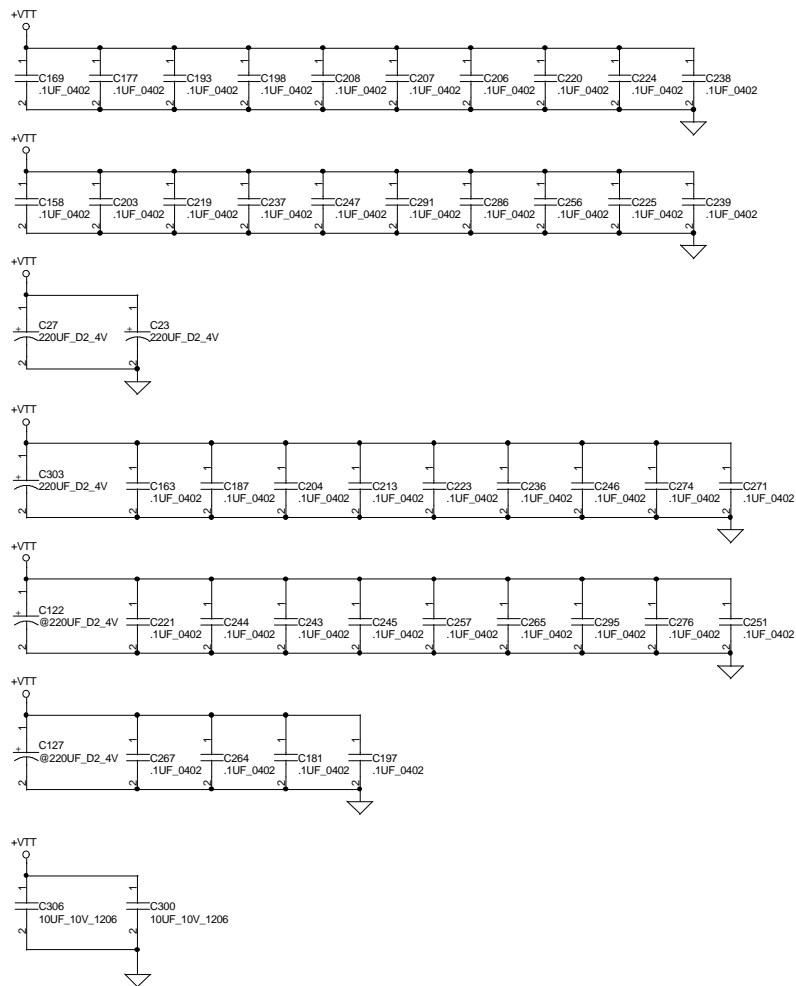






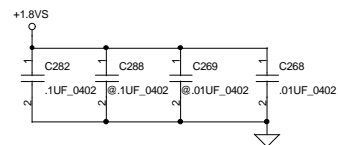
Layout note :

Distribute as close as possible
to GMCH Processor Quadrant .



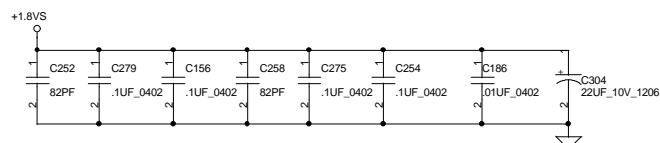
Layout note :

Distribute as close as possible
to VCCPCMOS_LM. (GMCH pin
AF6, AE7, AC9, AC8)



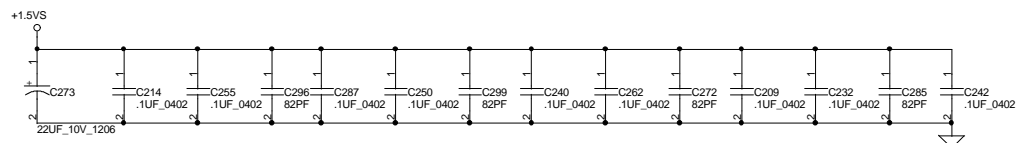
Layout note :

Distribute as close as possible
to GMCH Local Memory Quadrant .



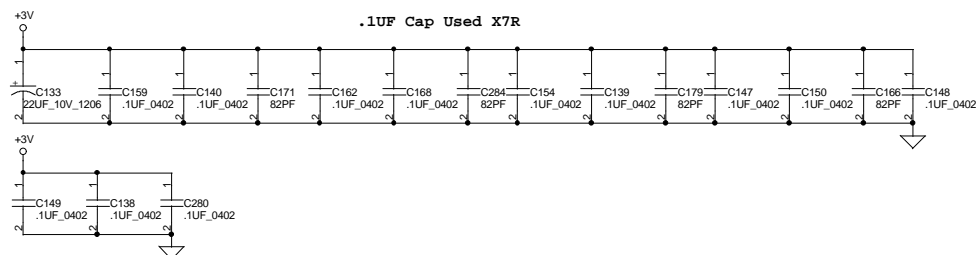
Layout note :

Distribute as close as possible
to GMCH AGP/DVO Quadrant .



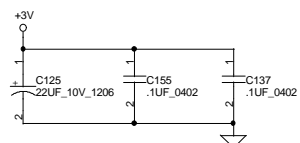
Layout note :

Distribute as close as possible
to GMCH System Memory Quadrant .



Layout note :

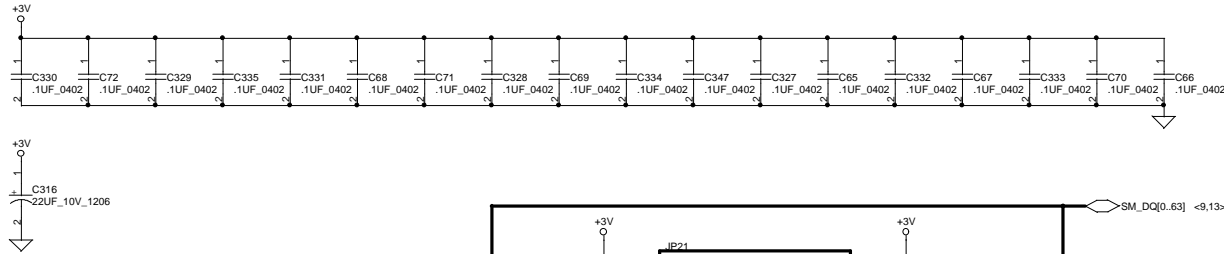
Distribute as close as possible
to IO Quadrant .



Compal Electronics, Inc.

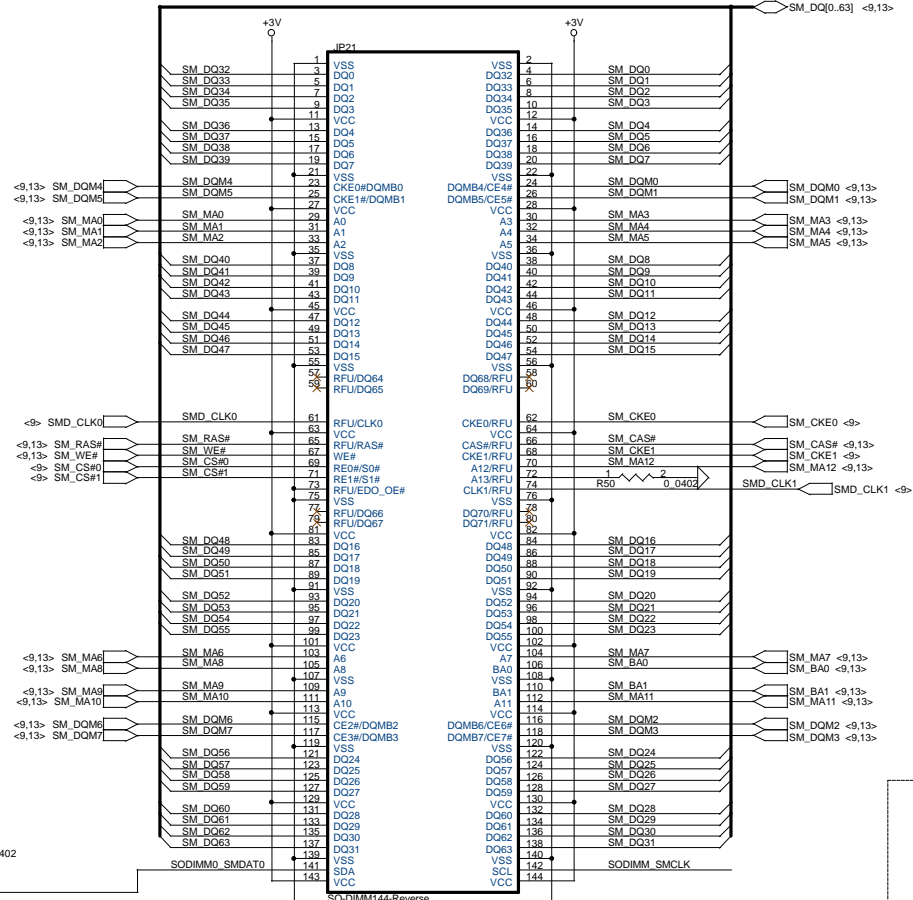
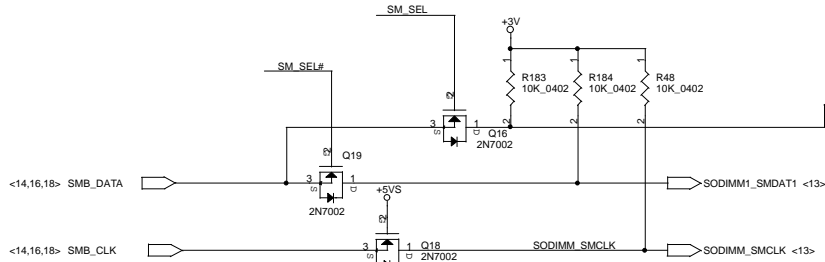
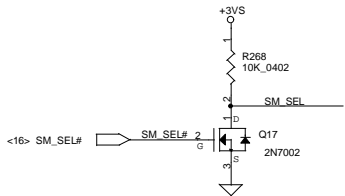
Title		GMCH-M Decoupling	
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Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



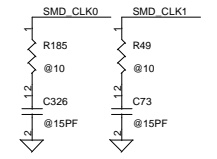
System S MBUS Select

SM_SEL#
0=SODIMM0 ;
1=SODIMM1



DIMM0

Place closely to DIMM0



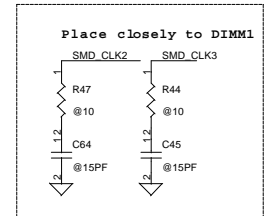
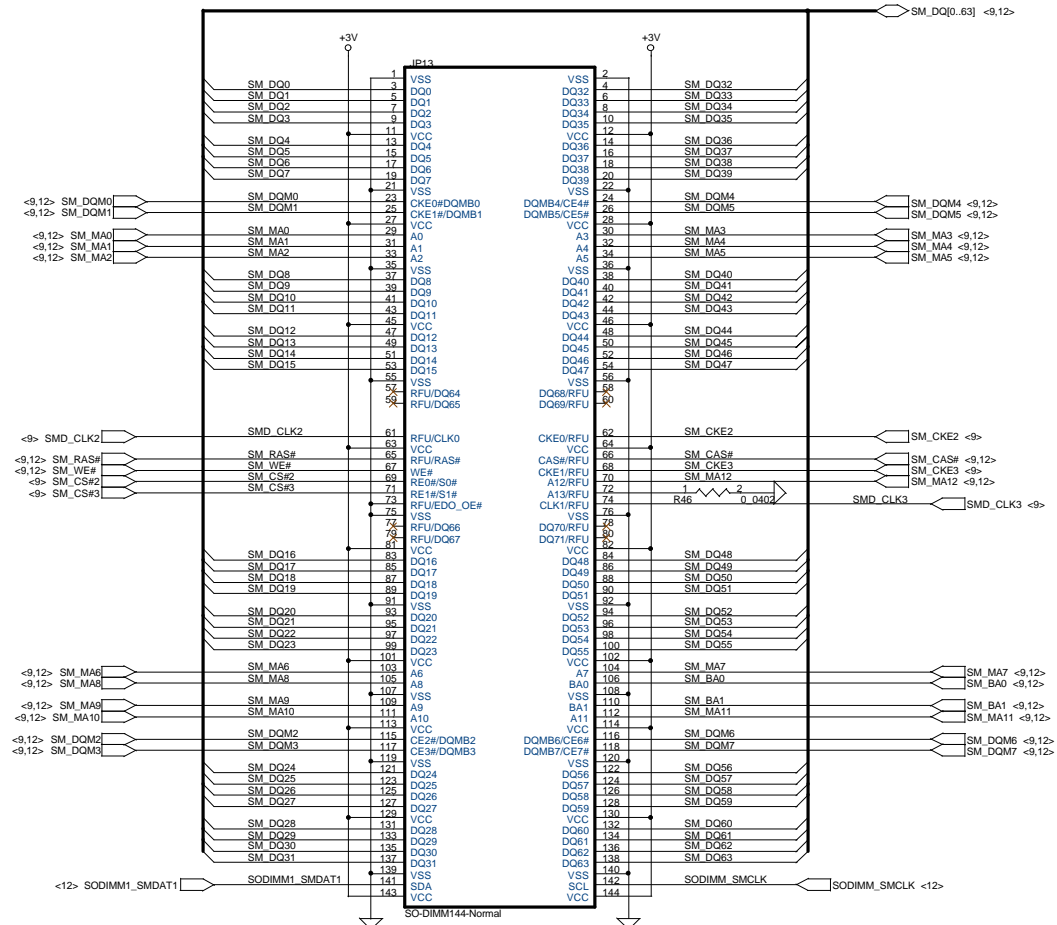
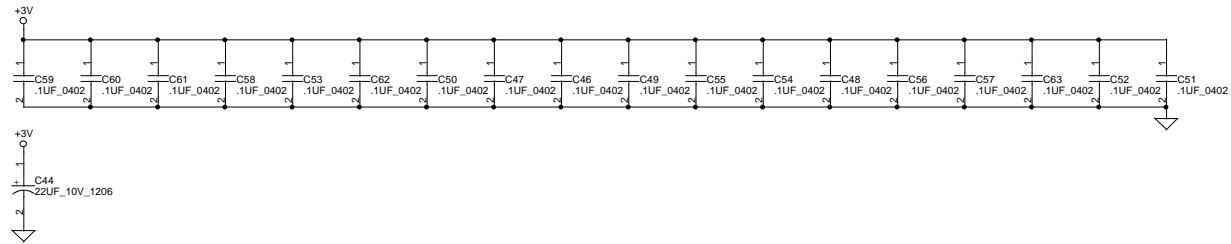
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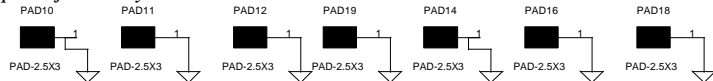
SO-DIMM SLOT0/Decoupling & DIMM Select

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Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM (DIMM 1) pin .



EMI Clip PAD for Memory Door



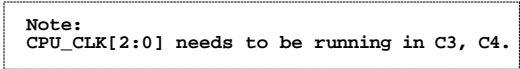
DIMM1

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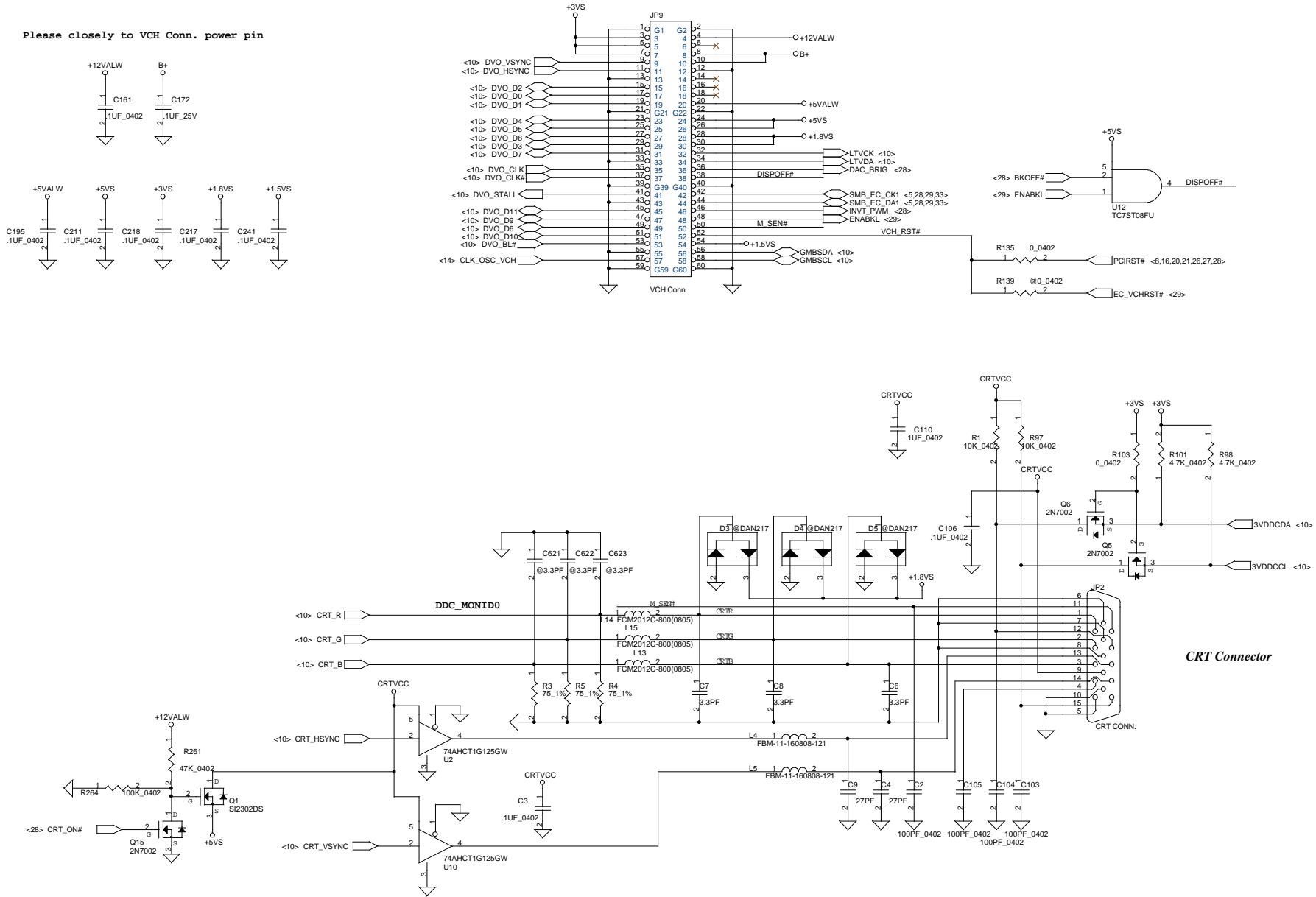
SO-DIMM SLOT1 & Decoupling

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Compal Electronics, Inc.			
Title			
Clock Generator			
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Please closely to VCH Conn. power pin

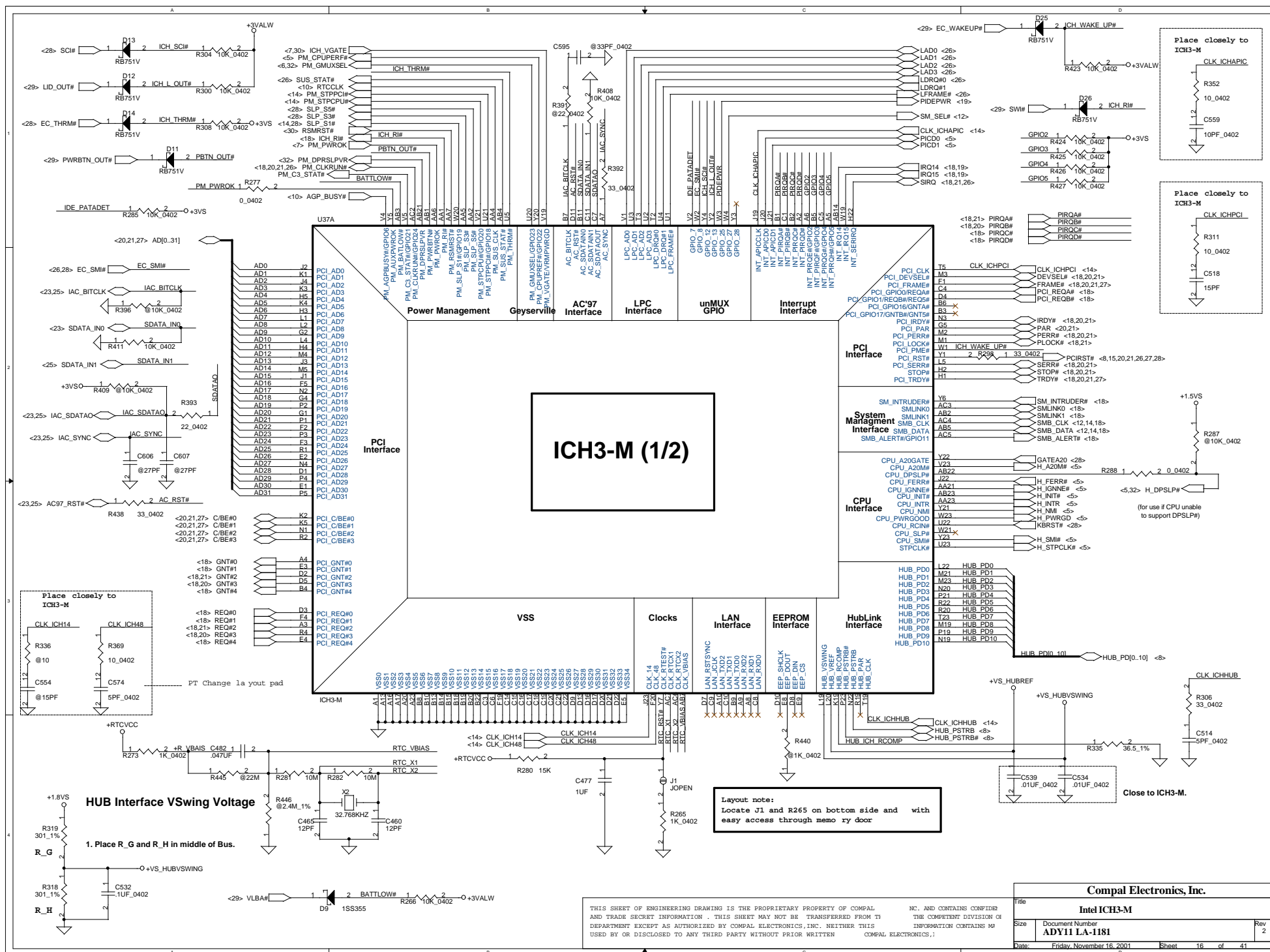


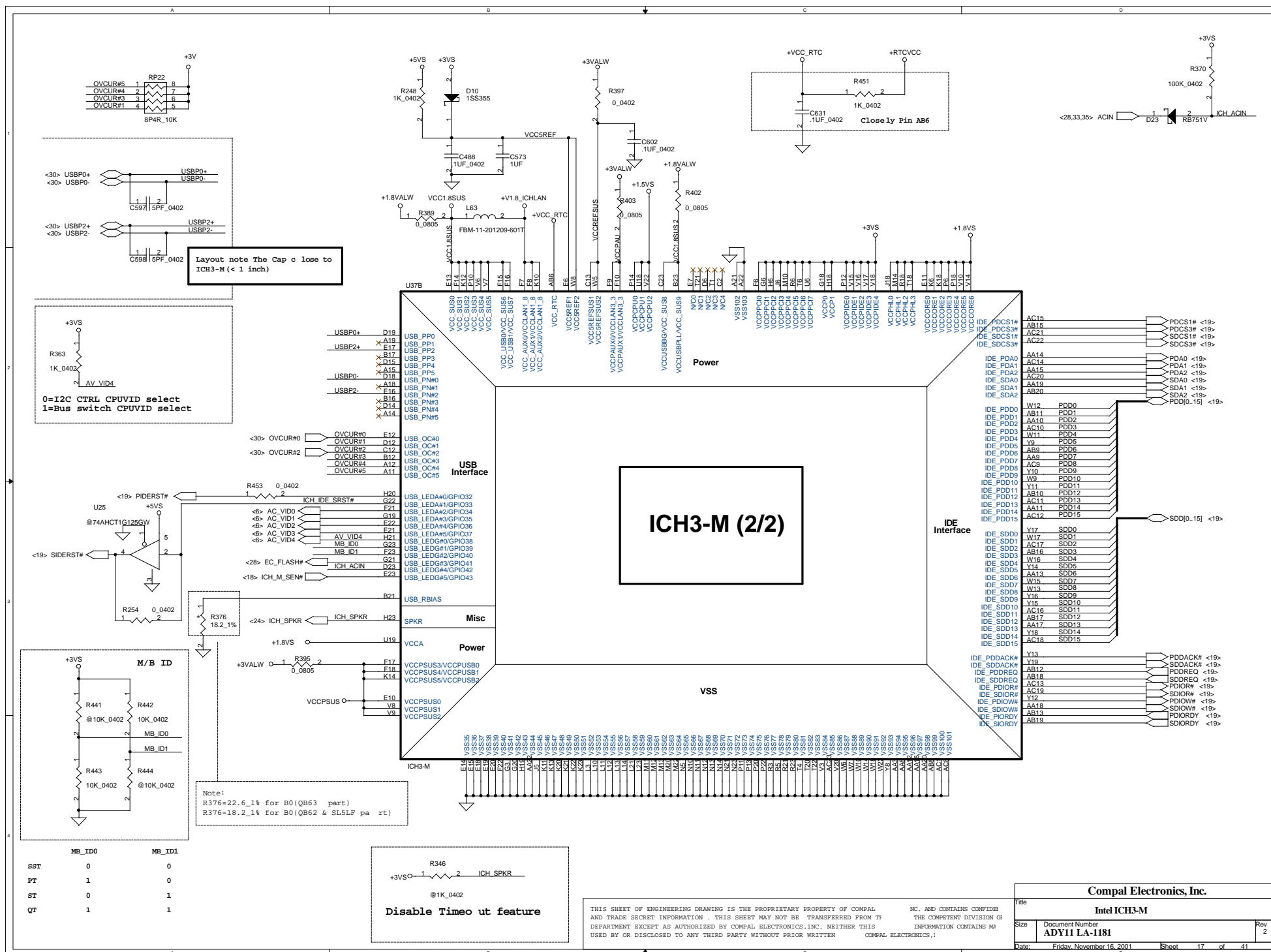
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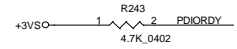
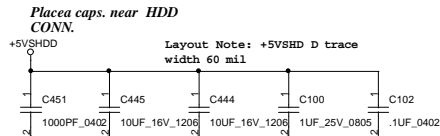
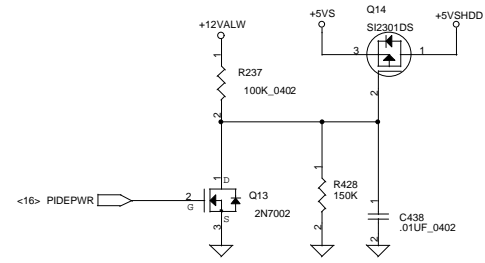
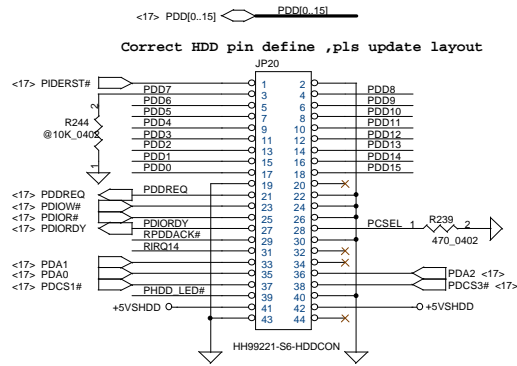
VCH Conn. & CRT

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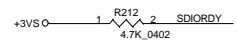
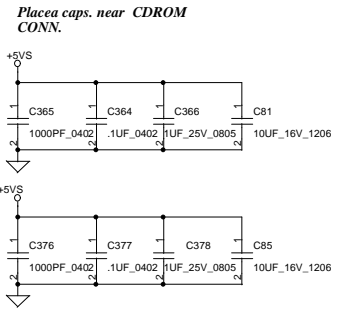
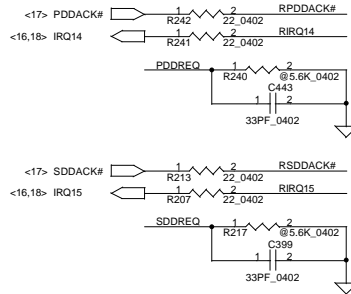
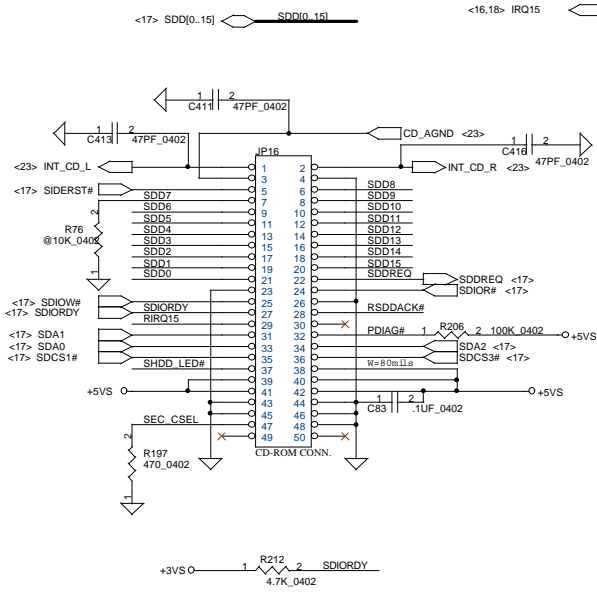




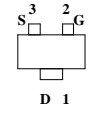
HDD Connector



CD-ROM Connector

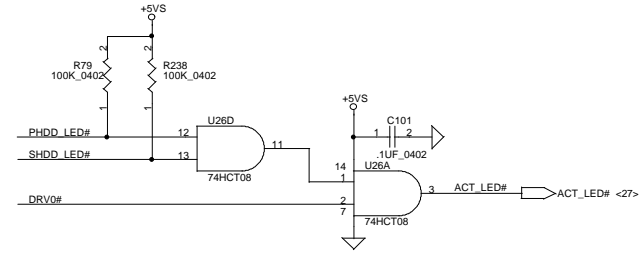
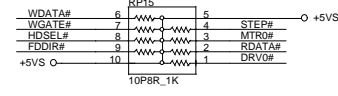
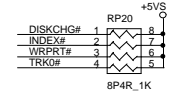
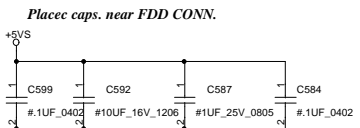
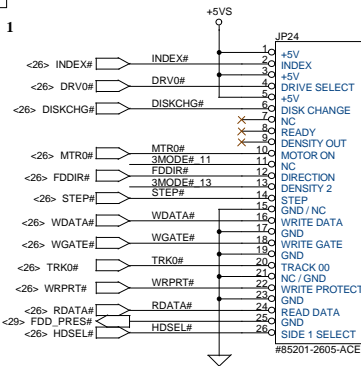


SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +8V



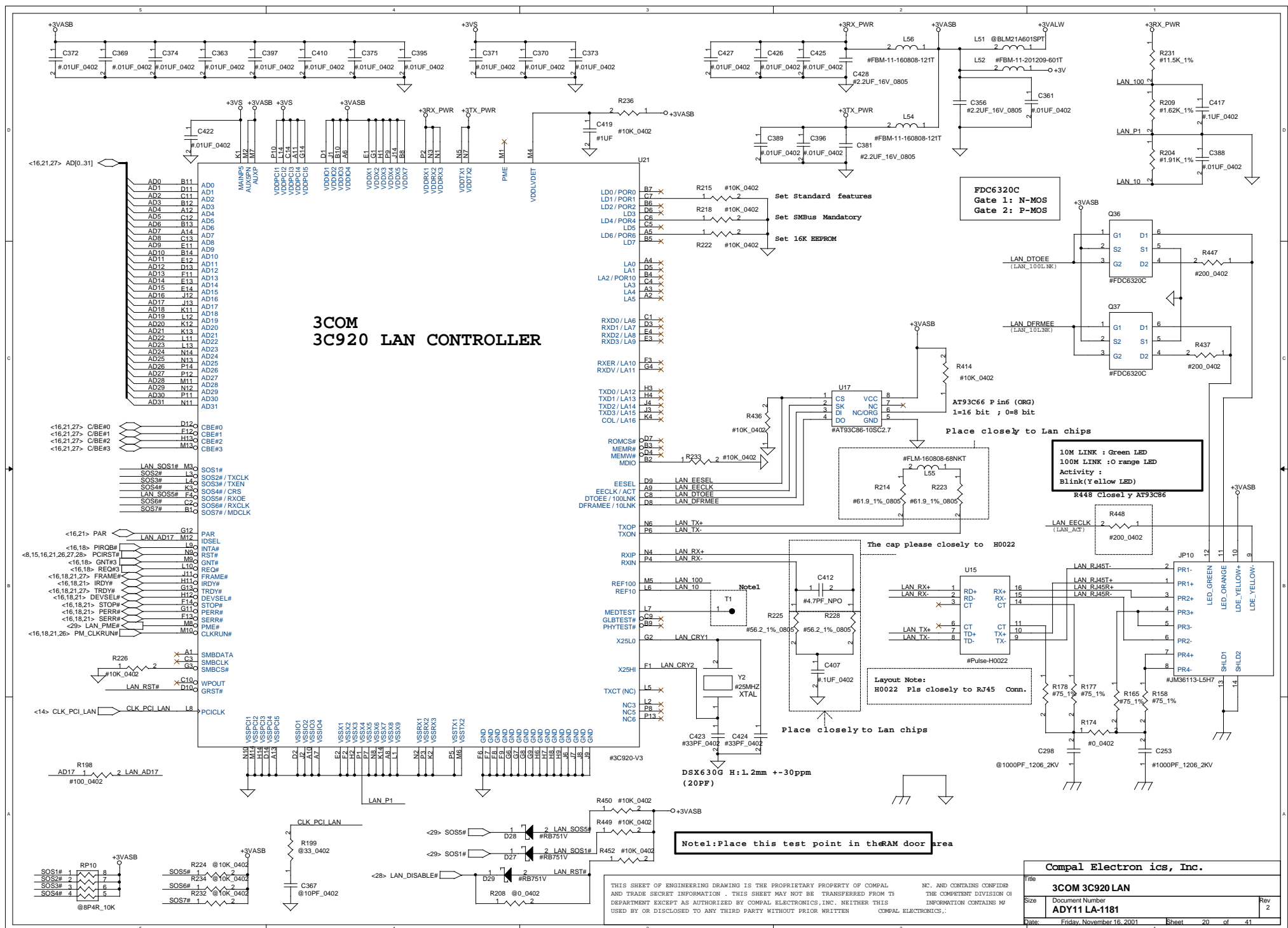
means no-pop for Tang
Note: PT-test must pop these component s

FDD Connector

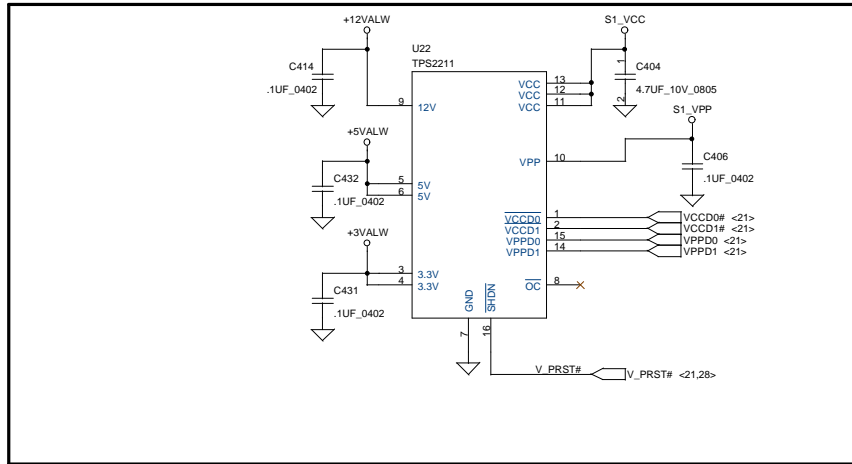


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Title IDE/FDD/CD-ROM Module		
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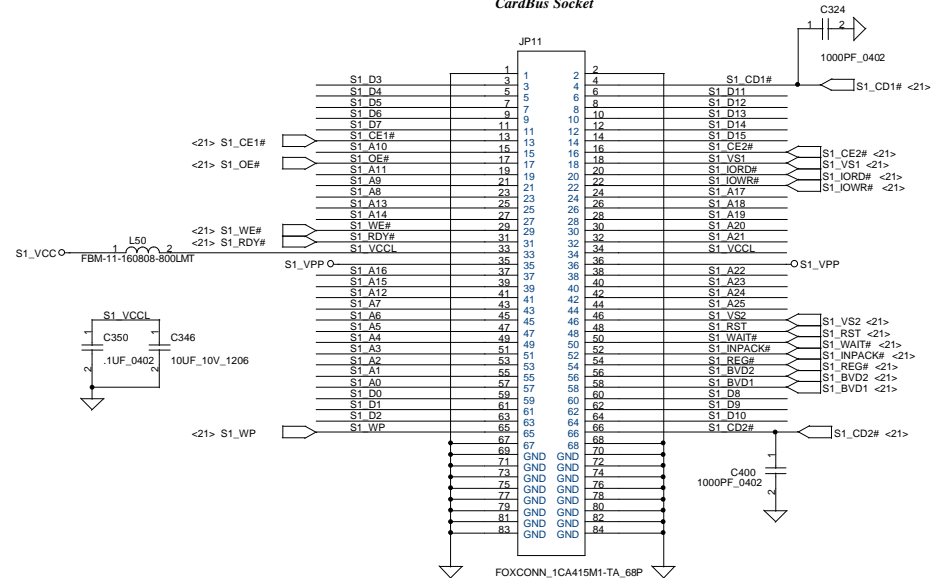


PCMCIA Power Controller



<21> S1_A[0..25]
<21> S1_D[0..15]

CardBus Socket

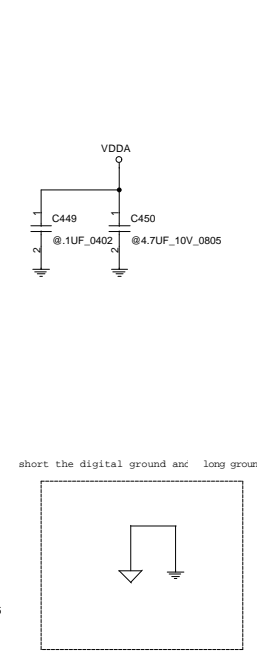
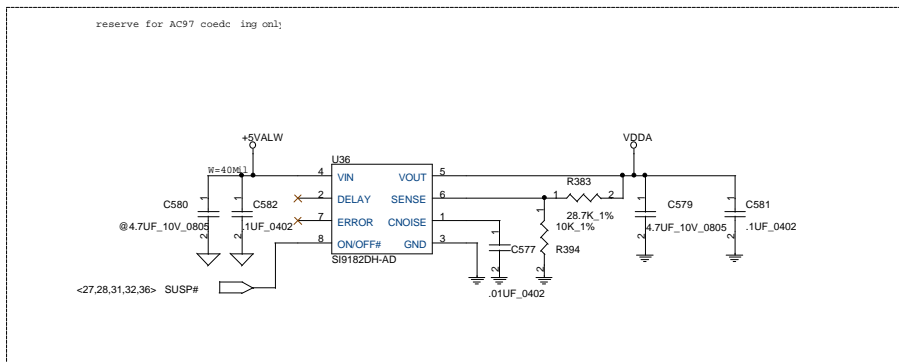


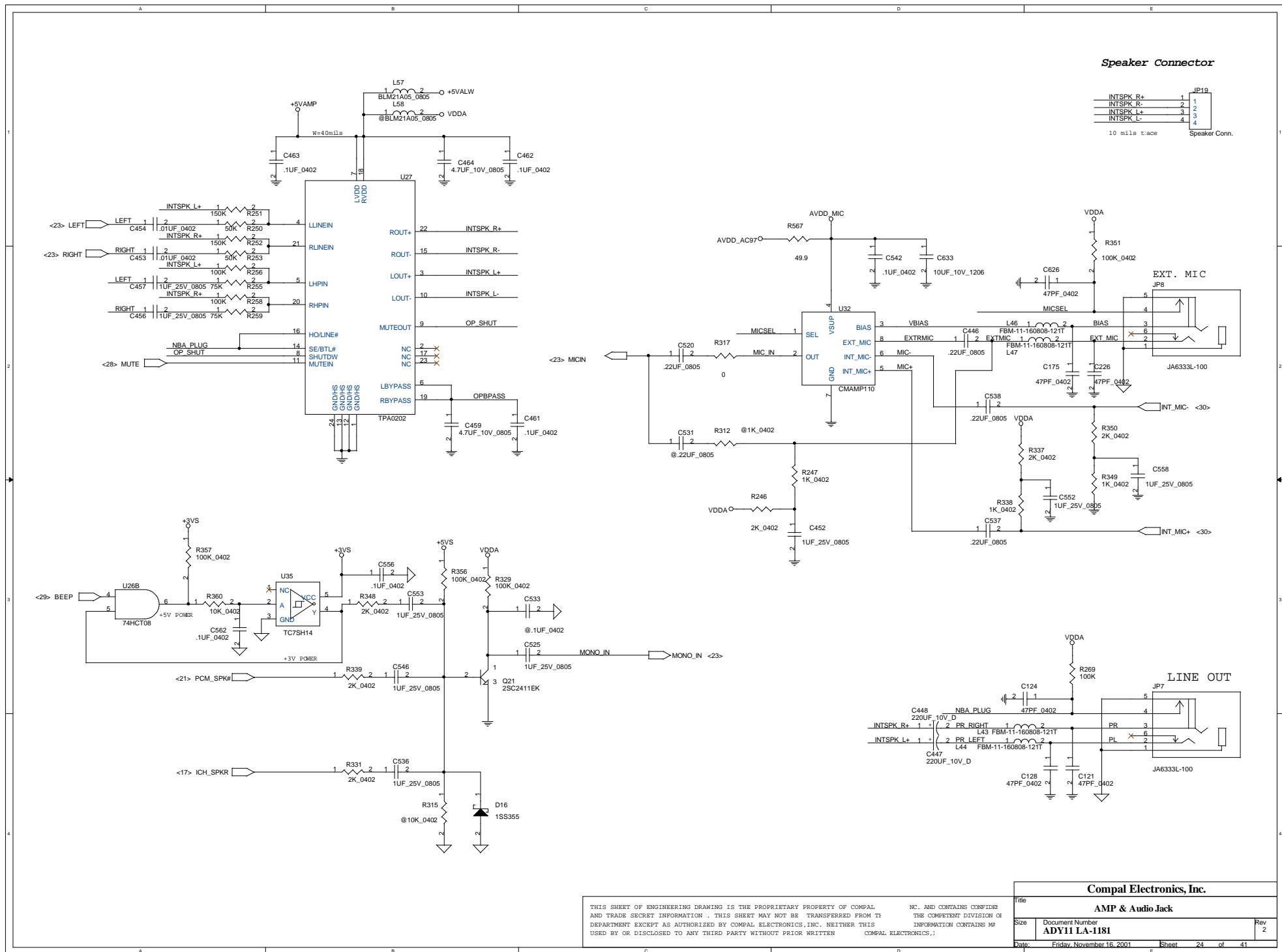
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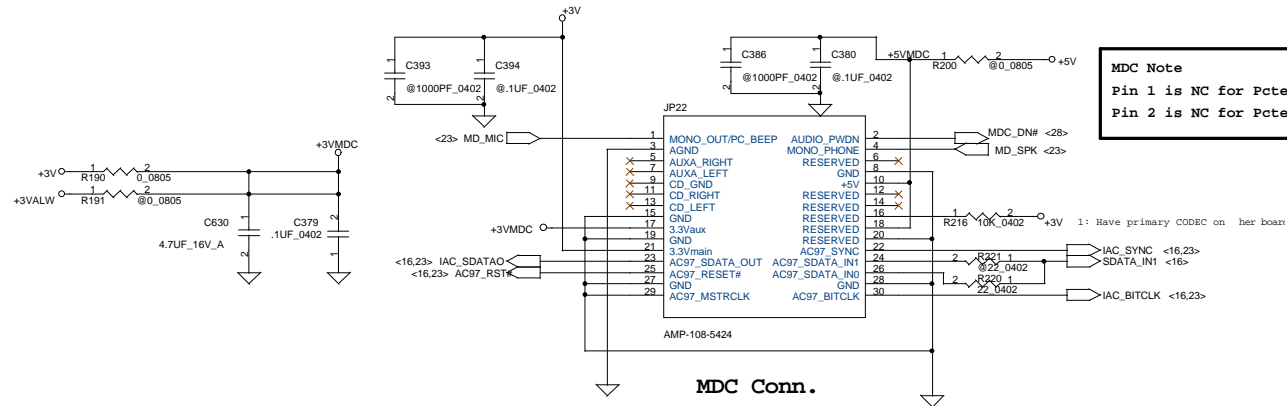
CardBus Socket

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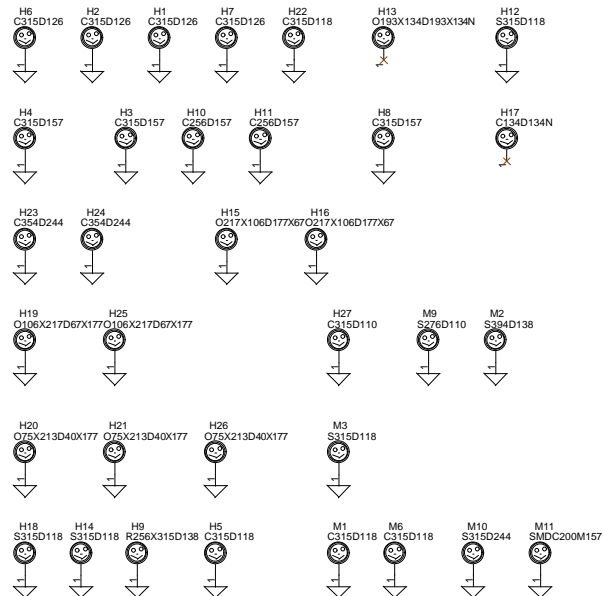


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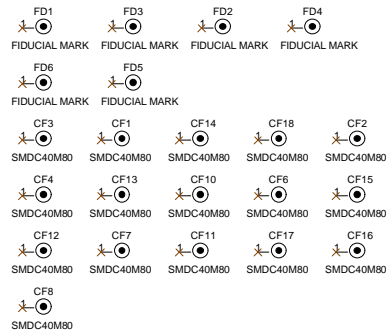


MDC Note
 Pin 1 is NC for Pctel and connexant MDC modem
 Pin 2 is NC for Pctel and connexant MDC modem

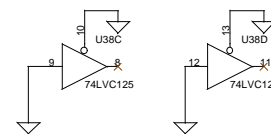
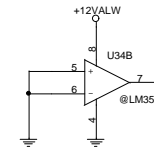
Screw Hole



Fiducial Mark

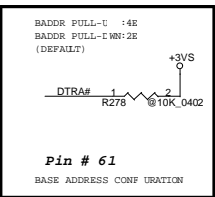


Spare Logic Gate



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Compal Electronics, Inc.		
Title		
MDC connector / Skew Hole		
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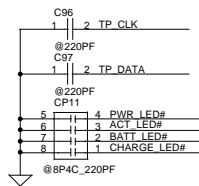
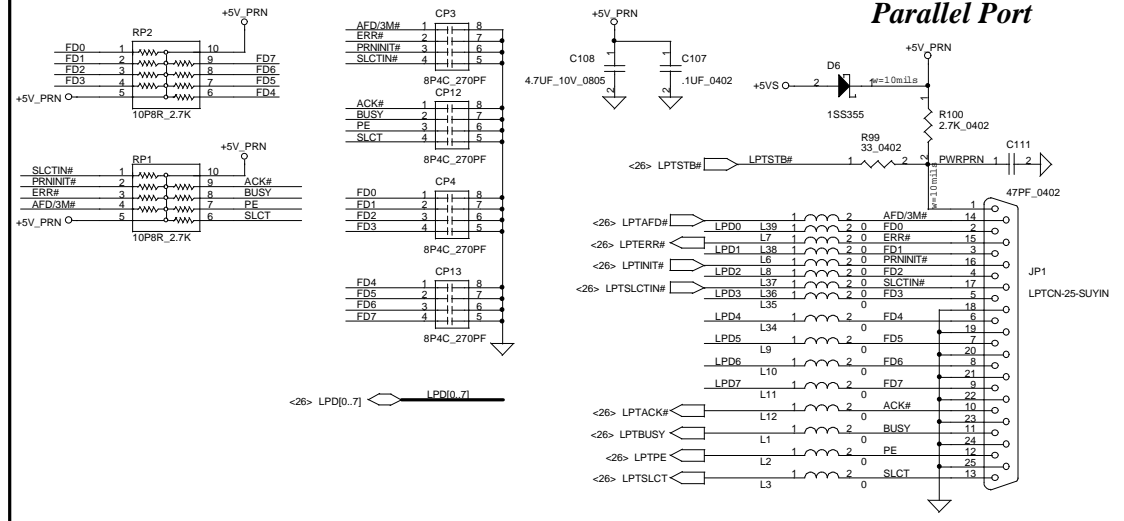
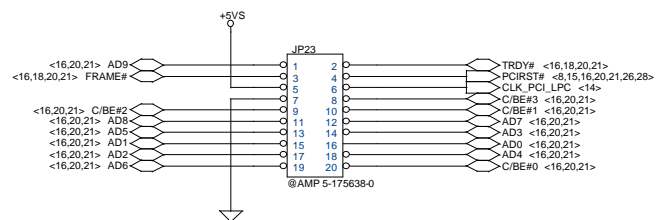


* 1 ROM SOLUTION

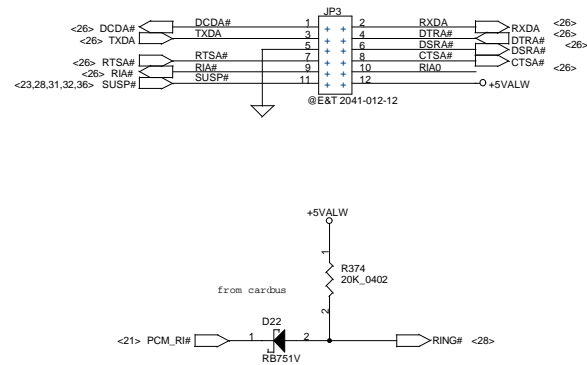
Pin connection diagram for JST BM20B-SRDS-G. The diagram shows a 20-pin connector with pins numbered 1 to 20. The connections are as follows:

- Pin 1: TP_CLK
- Pin 2: TP_DATA
- Pin 3: +5VS
- Pin 4: PWR_LED#
- Pin 5: BATT_LED#
- Pin 6: +5VALV
- Pin 7: PWR_LED#
- Pin 8: BATT_LED#
- Pin 9: +5VALV
- Pin 10: BATT_LED#
- Pin 11: +3VALV
- Pin 12: LID_SW#
- Pin 13: TP_CLK
- Pin 14: TP_DATA
- Pin 15: +5VS
- Pin 16: PWR_LED#
- Pin 17: BATT_LED#
- Pin 18: +5VALV
- Pin 19: PWR_LED#
- Pin 20: BATT_LED#

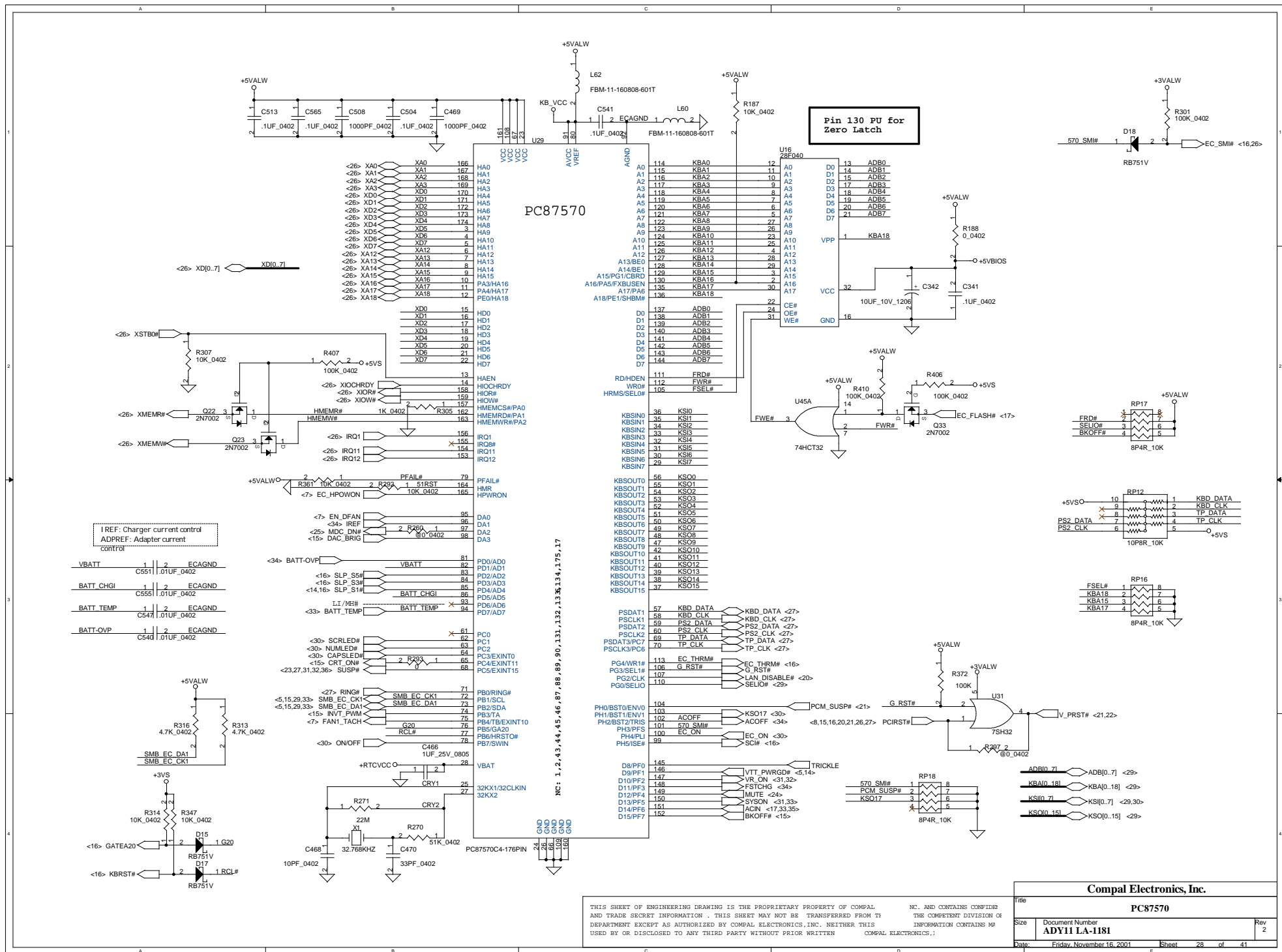
The diagram also shows connections for TP_CLK, TP_DATA, +5VS, +5VALV, +3VALV, LID_SW#, PWR_LED#, and BATT_LED#.



[illegible]

S/W debug only

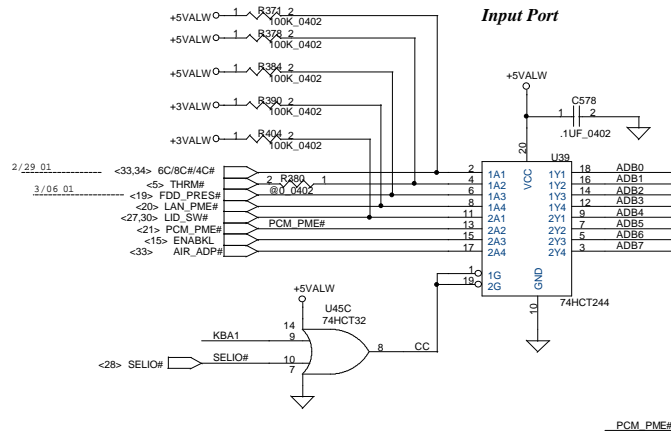


ACPI Debug port

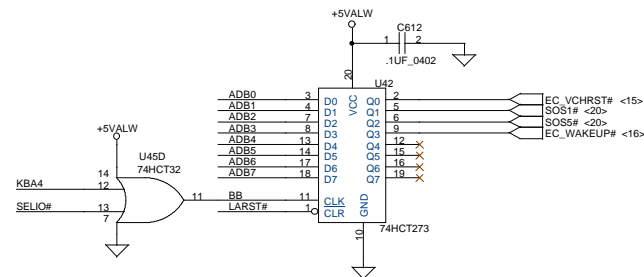
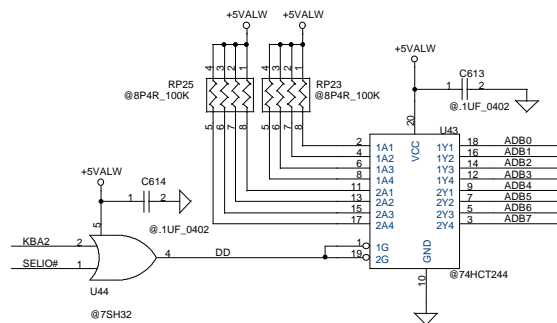
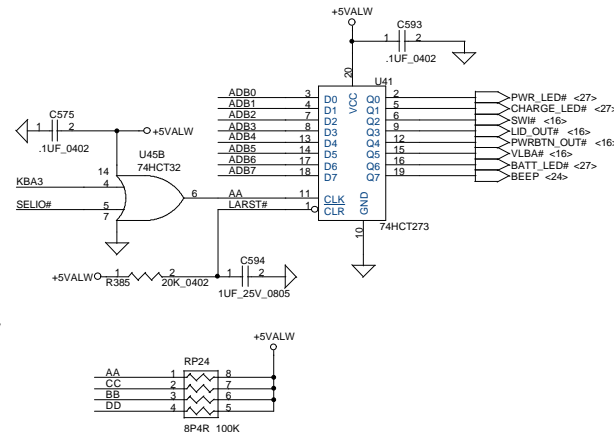




<28> ADB[0..7]  ADB[0..7]
<28> KBA[0..18]  KBA[0..18]

Input Port

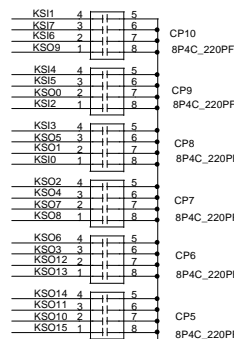
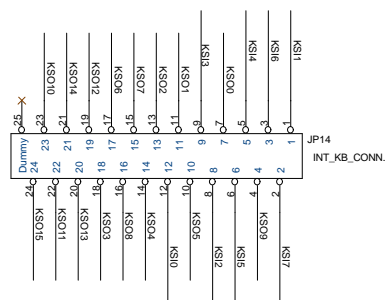


Output Port

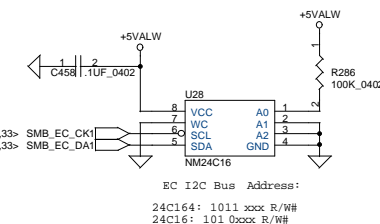


<28> KSO[0..15]  KSO[0..15]
<28,30> KSI[0..7]  KSI[0..7]

INT_KBD CONN.



NM24C164 Address definition: 1 A2 A1# A0 B2 B1 B0 R/W#



EC I2C Bus Address:
24C164: 1011 xxxx R/W#
24C16: 101 0xxxx R/W#

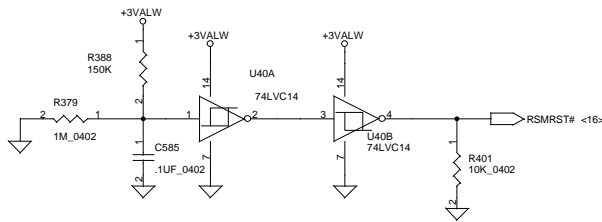
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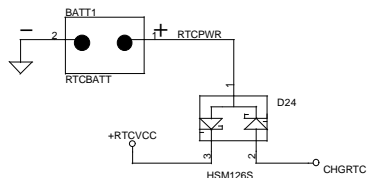
EC Extend I/O KB Conn. & BIOS

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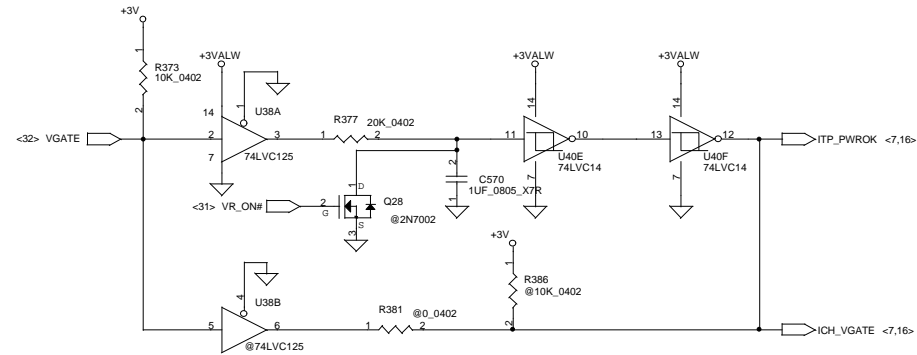
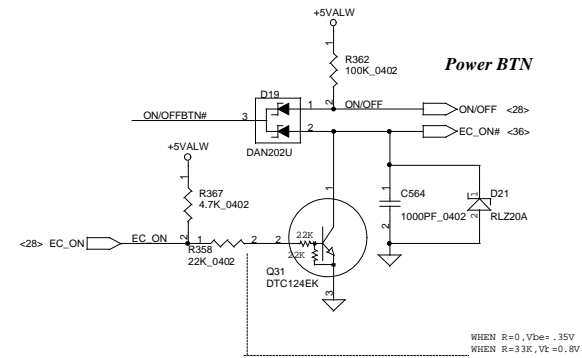
Power ON Circuit



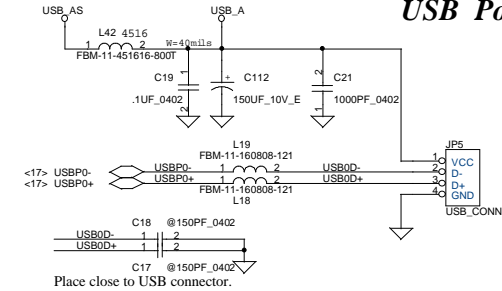
RTC Battery



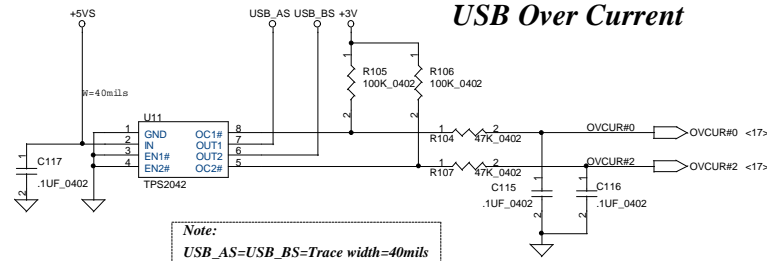
Power BTN



USB Port 0

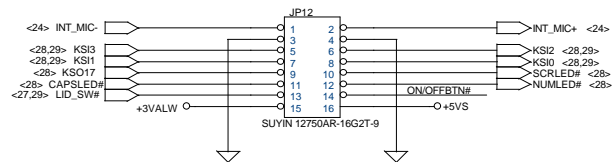


USB Over Current

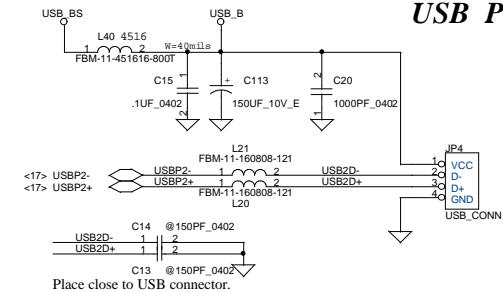


Note:
USB_AS=USB_BS=Trace width=40mils

LID Switch & Function Button



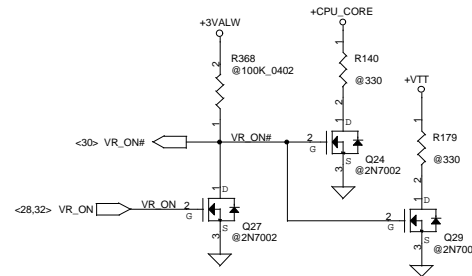
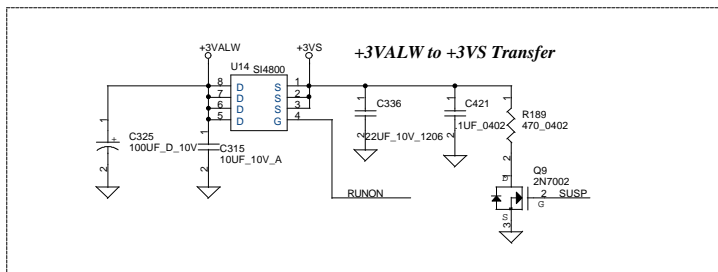
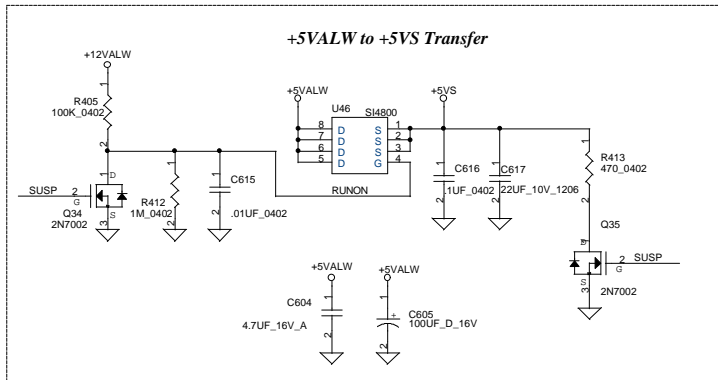
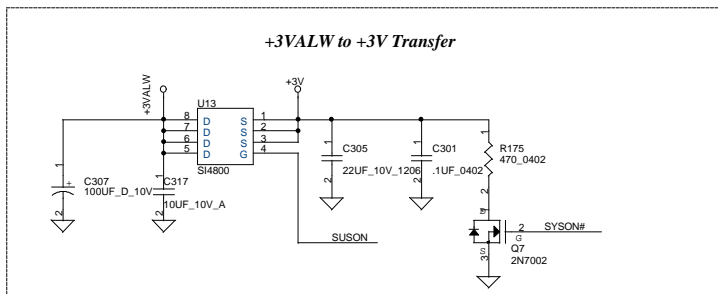
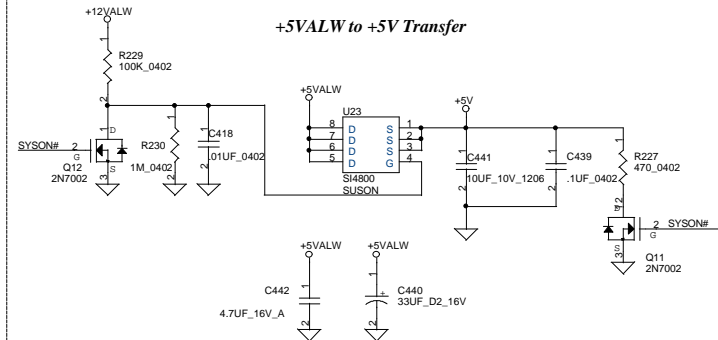
USB Port 1



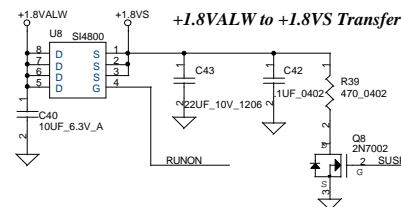
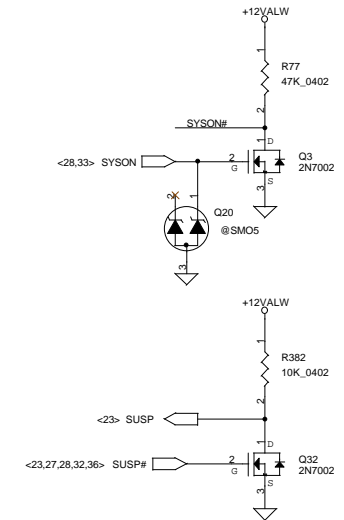
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Title		
Power OK/Reset/RTC battery/USB Conn.& Lid Switch		
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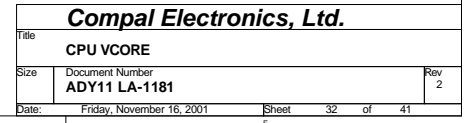
1.8VALW/+1.5VS Power direct provide



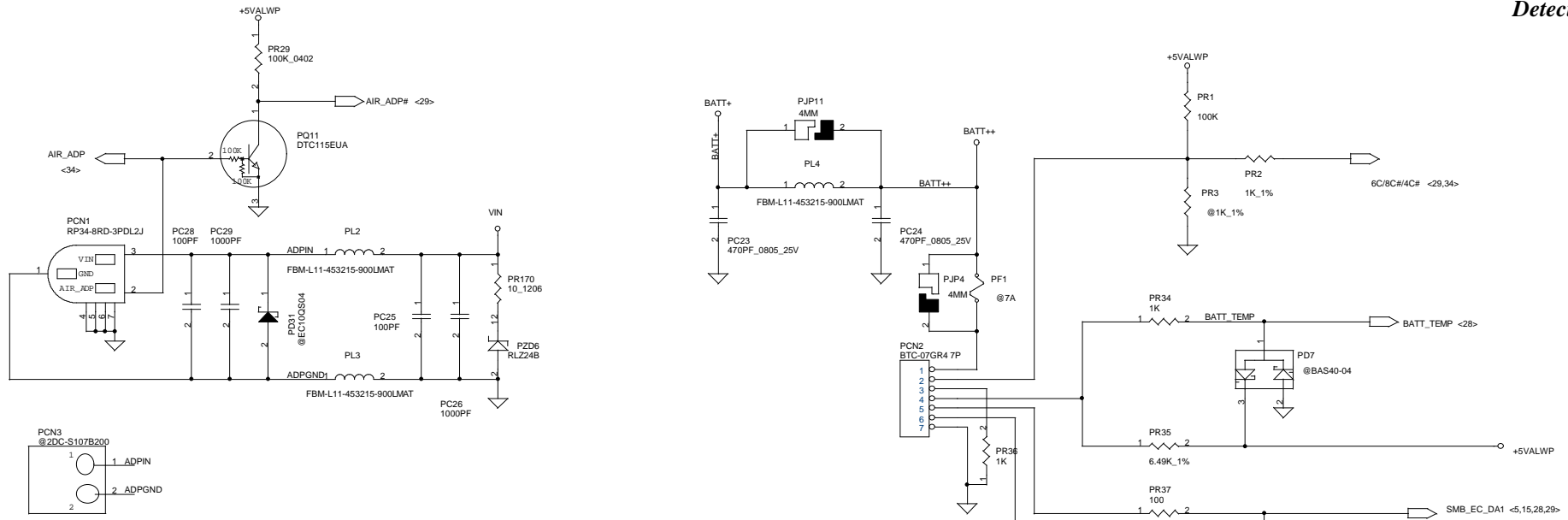
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Compal Electronics, Inc.			
Title	DC/DC Circuit		
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CPU-CORE/VTT

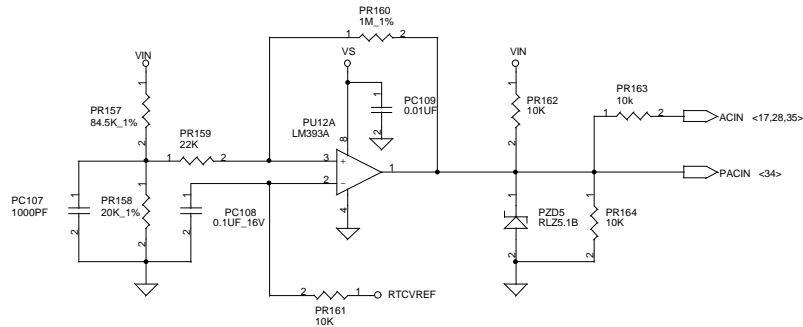


Detector

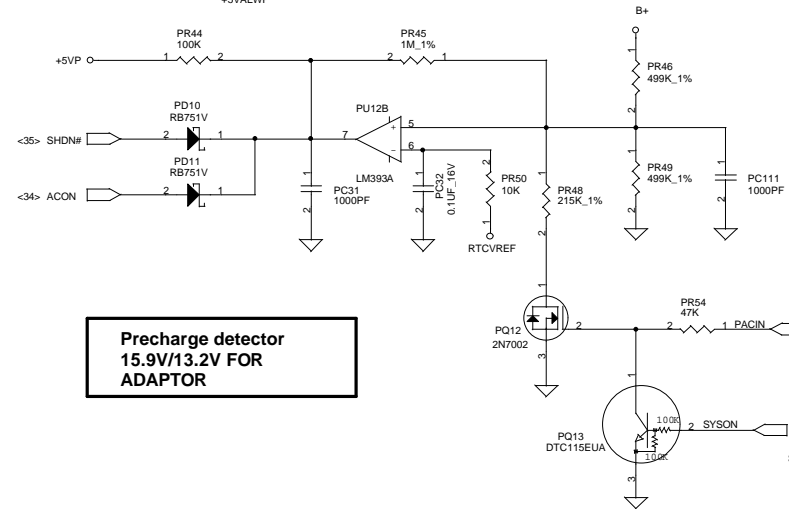


PCN2 battery connector pin assignment
 SMART Battery:
 1.BAT+
 2.LI/MH#
 3.B/I
 4.TS
 5.SMB_EC_DA1
 6.SMB_EC_CK1
 7.GND

**Vin Detector
 17.93V/17.2V**



**Precharge detector
 15.9V/13.2V FOR
 ADAPTOR**



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Compal Electronics, Inc.		
Detector		
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Charger

$I_{adp}=0\sim 3.07A$
 $I_{air}=0\sim 2.26A$

$I_{REF}=1.746 \cdot I_{charge}$
 $I_{REF}=0\sim 5V$

Charge voltage
 4S LI-ION
 NI-MH : 17.00V
 3S LI-ION : 12.75V

OVP voltage :

LI-4S : 18.0V---BATT-OVP = 3.97V

LI-3S : 13.5V---BATT-OVP = 2.98V

BATT-OVP=0.2 206*BATT++

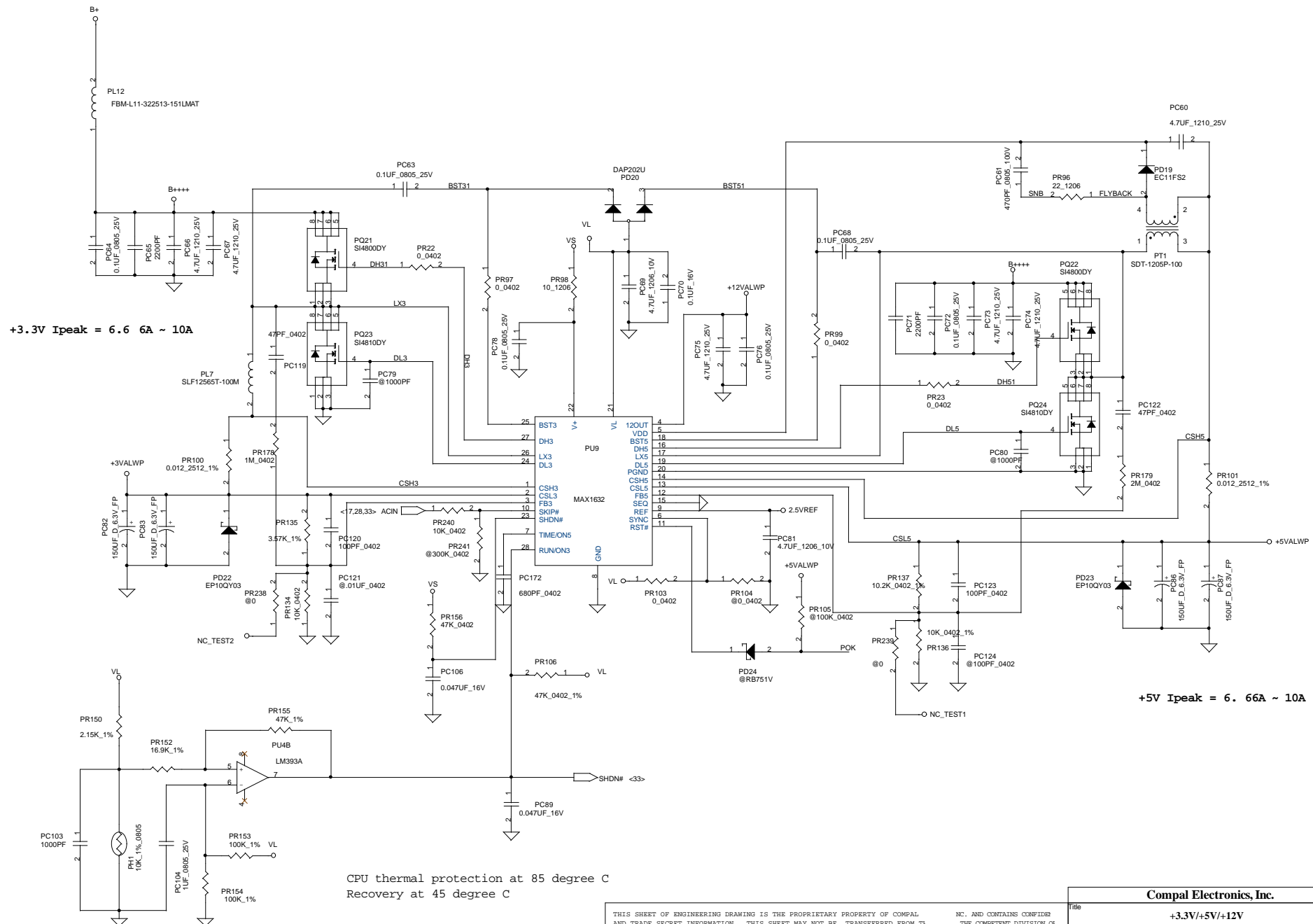
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Compal Electronics, Inc.

Charger

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+3.3V/+5V/+12V



CPU thermal protection at 85 degree C
Recovery at 45 degree C

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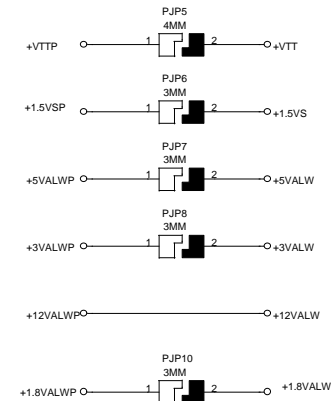
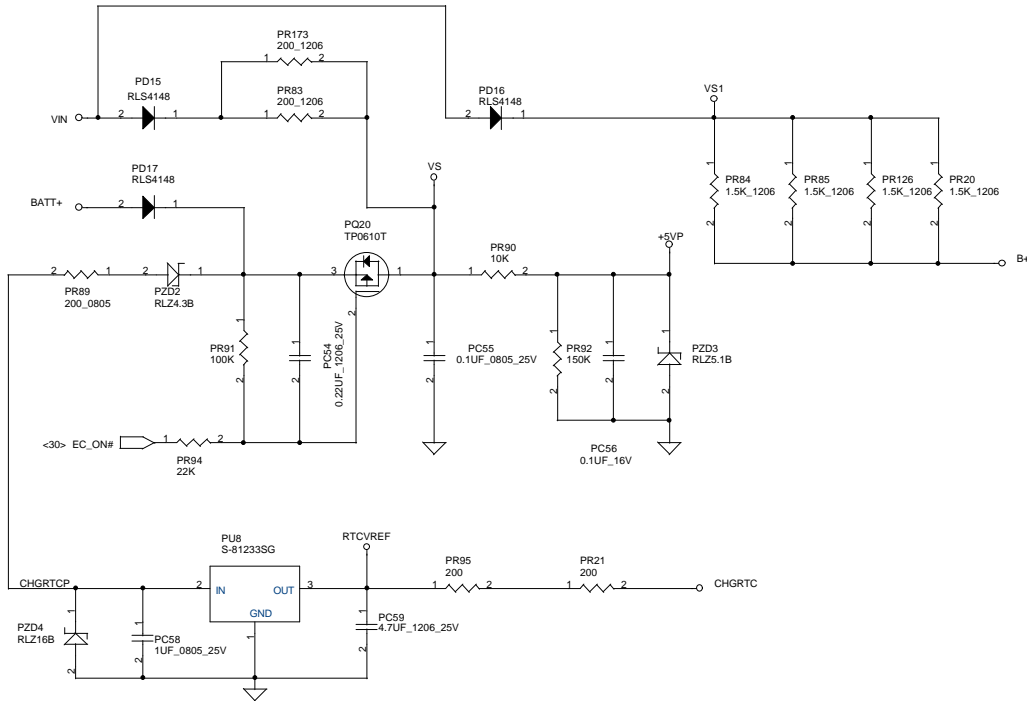
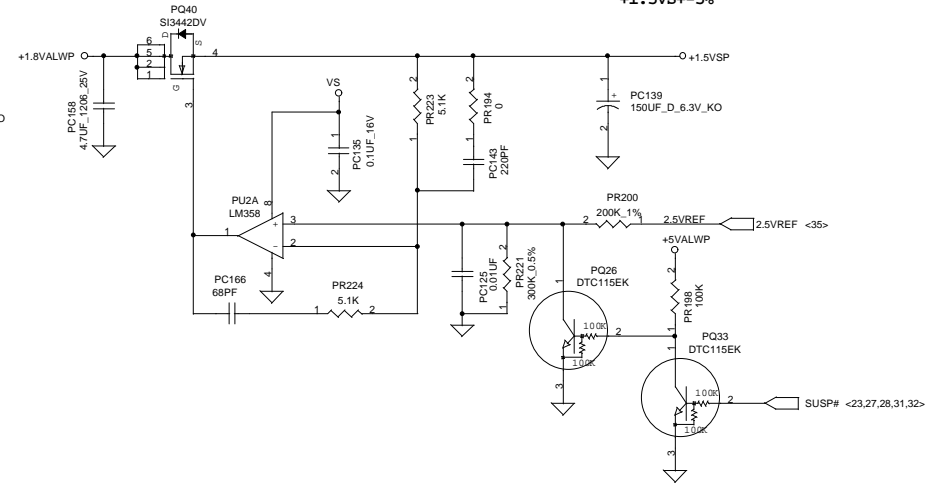
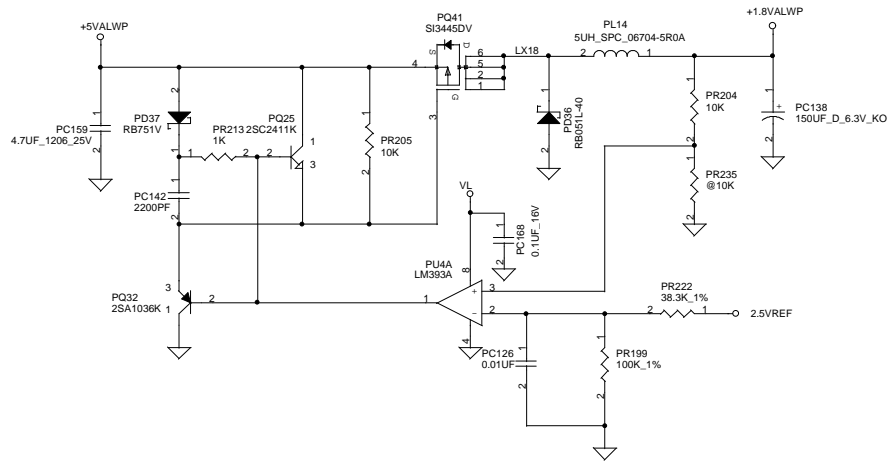
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+3.3V/+5V/+12V

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+1.8VALW/+1.5VS

+1.8V+-5%



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+1.8VALW

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B. Ver#	Phase
1	Core-logic Chipset revision	Revision error	0.1B	3	FW82810M should be QB88 and FW8280 1CAM should be QB63	0.1	SST
2	Leakage issue	+5VSHDD is on when plug AC-in and OS enter S3,S4,S5. we used GPIO25 of ICH3-M to control IDE power, but this pin is resume plane, keep high after RSMRST#.	0.1B	19	Q14 pin3 change from +5VALW to +5V S power plan	0.2	SST-2
3	Leakage issue	+5VS has about 500mv backdrive on S3;U2 6 is +5VS but pin9 pull up to +3V	0.1B	7	R94 pull up change to +3VS	0.2	SST-2
4	Leakage issue	+3VS has about 253mv backdrive on S3;Q 16 is on when S3	0.1B	12	R268 pull up change to +3VS	0.2	SST-2
5	Leakage issue	+3VS has about 253mv backdrive on S3;U37 pinU5 (ICH_THRM#) is +3VS plane	0.1B	16	ICH_THRM# pull up change to +3VS	0.2	SST-2
6	SM_CLK/DATA read and program failed	Signal connection error	0.1B	14	Correct net, U9 pin29 should be connected to SMB_DATA U9 pin30 should be connected to SMB_CLK	0.2	SST-2
7	Level shift	U26 is +5V output, but ICH3(U37) pinAA 6 is 3V level	0.1B	7	Change R415 from 100_0402 to 5.6K_04 02;BOM change	0.1	SST
8	Correct Part value	BOM and schematic value different	0.1B	19 20	Change JP20 value from "HH9927-S6" to "HH9921-S6" Change JP10 value from "JM361 13-L1H" to "JM36113-L5 H7"	0.1	SST
9	None	Original design, EC_FLASH control by IC H3-M GPIO40 or 97338 pin 71. Follow compal common design, use ICH3-M GPIO40 control EC_FLASH#.	0.1B	27	Change U33(97338) pin7 1 to NC	0.2	SST-2
10	VR_ON control	For EC can control VR_ON after VT_T_PWRGD# on	0.1B	29	VTT_PWRGD# connect to U2 9 pin146	0.2	SST-2
11	Debug card	Design change used PCI port 80 debug card solution	0.1B	28	Change JP23 connector type from "SHYI N 12793-10Q2" to "AMP 5-175638-0";BOM change	0.2	SST-2
12	None	FAN power transistor change. Max. power of 2 SC2411 is 0.2W. Max. power of FMMT619 is 0.615W.	0.1B	7	Change Q4 from "2SC2411EK" to "FMMT619" BOM change	0.2	SST-2
13	Component pad size	Component is 0402 size, but layout pad size is 0603	0.1C	17	Layout modified and correct value from "5PF" to "5PF_0402";BOM needn't change	0.2	SST-2
14	Mechanical limit issue	Mechanical limit H:2.2mm, used component over limit	0.1C	32	Change C440 from "100UF_D_16V" to " 33UF_D2_16V" D2 size H=1.9mm; BOM change	0.2	SST-2
* 15	Delect item 11	PT implement PCI port 80 solution	0.1C	28	SST2 don't change	0.2	SST-2
16	Clock waveform	Clock waveform over SPEC 1. CLK_HCLK/H CLK# 2. CLK_DR EF 3. CLK_ICHA PIC	0.1C	14 16	1. Change R16, R12 from "33_1%" to "10_1%" 2. Change R59 from "22_0402" to " 10_0402" 3. Pop R352 (10_0402) and pop C559 (10PF_04 02)	0.2	SST-2
17	None	LPC debug card on developer stage , depop it.	0.1C	28	Depop JP23 (S SST2)	0.2	SST-2
18	Correct Part value	BOM and schematic value different	0.1D	24	Change R383 value from "29K_1%" to "28.7K_1%"	0.1	SST
19	Fixed EE issue list item11(2001/6/5)	Intel recommend series resistor on IDERST	0.1D	17	Add R453(0_0402) series resistor on PIDERST #--- BOM modify	0.2	SST-2
20	Fixed EE issue list item10(2001/6/5)	VCCA_DAC should have a 0.1uf and 0 .01uf nearby	0.1D	10,11	We check layout file, C290 closely U7 pin AF26, so change C290 from pag11 to pag10, C156 and C 186 change to page 11(not change layout), and add C632 [0.01UF_0402] near AF 26	0.2	SST-2
21	Fixed EE issue list item26,27(2001/7/12)	1. Change CPU thermal skew hole size change. 2. CD-ROM skew hole size change.	0.1D	26	1. Change H1, H2, H6, H7 from 2.8mm to 3.2mm 2. Change H9 from 3.5mm long by 3.0mm wide	0.2	SST-2
* 22	CLK_HCLK/HCLK# resistor need n't change	Follow Dell's recommend	0.1E	14	R12, R16 resistor to restore, de 1 item16-1	0.1	SST
23	ICH3 revision	SST2 used QB62 or SL5LF revision	0.1E	17	Change R376 from "22.6_1%" to "18.2_1%" , BOM already change OK.	0.2	SST-2
24	CLK EMI issue	Add AC termination on as below signals 1. CLK_GB IN 2. CLK_ICHH UB 3. CLK_ICH 48 4. CLK_PCI_S IO 5. CLK_GBO UT 6. CLK_ICHP CI	0.1F	8 16 27 14 16	1. Pop R168(33_0402) and C297(5PF_0402) 2. Pop R306(33_0402) and C514(5PF_0402) 3. Pop R369(10_0402) and C574(5PF_0402) 4. Pop R324(10_0402) and C543(5PF_0402) 5. Pop R69(33_0402) and C92(1 0PF_0402) 6. Pop R311(10_0402) and C518(15PF_0402)	0.2	SST-2
25	None	Gerber release	0.2		Change Schematic revision to 0.2	0.2	SST-2

Compal Electronics, Inc.

Title

P.I.R History

Size

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2

Date:

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Sheet

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B. Ver#	Phase
26	None	Connector change	0.2A	19	FDD Connector change to ACES 85201-2605	0.3	PT
27	None	Remove OZ6933 PCMCIA Controller	0.2A	21 25	1. Del Page 21, and shift down page 2. Del CF5, CF9	0.3	PT
28	None	Remove Power Switch (2 slot) and change CardBus Connector	0.2A	22	1. Schematic remove U20, C437, C403, C402, C436, C434, C433, C415, C408, C429, R219, R211, C79, C80, C430, C318, L53, C358, C343, C401 2. Change PCMCIA Socket value to FOXCONN 1CA415M1-TA	0.3	PT
29	None	Add Board_ID for check Mosaic and Tang	0.2A	26	Add U33 Pin71 for BOARD_ID, and Add Resistor R565 10K_0402 and R566 0_0402	0.3	PT
30	None	Remove Serial Port	0.2A	27	De-pop C1, C5, C10, C11, C109, U1, JP3, CP1, CP2, L26, L27, L28, L29, L30, L31, L32, L33, Q26.	0.3	PT
31	None	Lid Switch function change to Touch-pad Board	0.2A	27	Schematic change, JP15 Pin17 net to +3VS, JP15 Pin18 net to LID_SW#	0.3	PT
32	None	Debug Port change connector	0.2A	27	Debug Port change connector from SUYIN 12793A-10G2 to AMP 5-17563 8-0	0.3	PT
33	None	Power on switch board change connector	0.2A	30	Power On switch board change from AMP 4-175638 to SUYIN 12750AR-16 G2T-9	0.3	PT
34	None	ICH_VGATE delay	0.2A	30	1. Schematic change, connect R381 pin2 to U40 Pin12 2. De-pop R386, R381	0.3	PT
35	None	Schematic remove Serial PORT function	0.2A	27	Schematic remove U1, CP1, CP2, C1, C5, C10, C11, C109, L26, L27, L28, L29, L30, L31, L32, L33, Q26.	0.3	PT
36	CMOSREF not strong enough to provide the target 2/3 ratio divider	Change divider to 0.5K/1K at the next available opportunity to gain more CMOSREF margin.	0.2A	5	BOM change R20 from 1K_1% to 499_1%, R22 from 2K_1% to 1K_1%	0.3	PT
37	None	M/B ID change to PT	0.2A	17	BOM add R441 10K_0402, Depop R443 10K_0402	0.3	PT
38	None	Gerber release	0.3		Gerber release, schematic change to 0.3	0.3	PT
39	Cost down	Core_VCC and VTT capacitor reduce.	0.3	6 11	1. BOM depop C126, C120, C293, C210, C283, C118. 2. BOM change from 150UF_D2 6.3V (45mOhm) to 220U_D2_4V(25mOhm), Location C29, C39, C32, C292, C260, C119, C153, C289, C37. 3. BOM depop C122, C127. 4. BOM change from 150UF_D2 6.3V (45mOhm) to 220U_D2_4V(25mOhm), Location C27, C23, C303.	0.3	PT
40	None	Remove Capacitor	0.3B	6	Schematic remove C120.	1.0	ST
41	None	Resistor Package error.	0.3B	24	Change R351 100K_0603 to R351 100K_0402	1.0	ST
42	Suspend from lid switch, can't resume from open LCD.	Change Lid switch power plan from +3VS to +3VALW.	0.3C	27 29 30	1. Schematic JP15 Pin.17 to +3VALW 2. Schematic JP12 Pin.15 to +3VALW 3. Schematic R404 Pin.1 to +3VALW	1.0	ST
43	For thermal module difference Mosaic-P4	Add stand-off on mother board.	0.3C	6	Schematic remove C39, add M11 S MDC200M157, BOM add C283 220U_4V_D2.	1.0	ST
44	None	Change Capacitor spec.	0.3C	31	BOM change C307, C325, C605 from 100UF_D_16V to 100UF_D_10 V.	1.0	ST
45	CRT connector layout shift.	Shift CRT connector 1.33mm	0.3C			1.0	ST
46	Factory DXF fix.	Layout modify.	0.3C			1.0	ST
47	Test point review.	Layout modify.	0.3C			1.0	ST
48	3COM 3C920 reference RJ45 version update.	VDDPCI[1:5] pins from +3VASB to +3VS.	0.3C	20	1. Schematic modify, U21 some pin change power plan from +3VASB to +3VS (VDDPCI [1:5]) 2. Schematic C370, C371, C373 change power plan from +3VASB to +3VS.	1.0	ST
49	Poor quality w/static noise on recording function.	Change MIC-AMP power plan.	0.3C	24	1. Schematic modify, MIC-AMP change power plan from VDDA to AVDD_MIC with R567 49.90hm to AVDD_AC97 2. Schematic add C633 10UF_10V_1206	1.0	ST
50	None	M/B ID change to ST	0.3D	17	BOM depop R441, R444, add R442, R443 10K_0402	1.0	ST
51	None	Change Back-light gate power plan.	1.0	15	1. U12 power plan from +3VS to +5VS. 2. U12 from SH08 to ST08		

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	CPU_CORE voltage is unstable	Change PWM frequency from 300KHz to 200KHz	0.1B	33	1.Change PR197 from 100 to 0 2.Connect pin10 of PU6 to pin9 of PU6	0.1	SST
2	+5VALWP is unstable	Change PWM frequency from 200KHz to 300KHz	0.1B	36	1.Delete PR104 and add PR103 0_0402 2.Connect pin15 of PU9 to ground	0.1	SST
3	Output capacitor of Charger interfere mechanical (switch board)	Change PC48 to small size,the height limited is 6mm in this area	0.1B	35	Change PC48 from 100UF to 68UF	0.2	SST2
4	The time sequency of +1.5VS is error	Change REF voltage from 2VREF of MAX1718 to 2.5VREF of MAX1632	0.1B	37	.Change PR200 from 100K_1% to 200K_1%	0.2	SST2
5	The time sequency between 1.8VALWP and 3.3VALWP is error	Delay 3.3VALWP start-up time	0.1B	36	Add PC172 680PF connected to pin7 of PU9	0.2	SST2
6	RTC battery that will be shortage.We changed RTC battery from Panasonic VL1220 to Maxell ML1220	Change LDO charger to 3.3V for Maxell ML1220 Modify Vin Detector and Precharger Detector circuit	0.1B	37 34	Change PU8 from S-81235SG to S-81233SG 1.Change PR157 from 78.7K_1% to 84.5K_1% 2.Change PR48 from 249K_1% to 215K_1%	0.2	SST2
7	Correct part vaule	BOM and schematic vaule different	0.1D	37	Change PL14 vaule from "5UH_SPC_06703" to "5UH_SPC_06704-5R0A"	0.1	SST
8	Correct current limited value	Modify current limited from 2.86A to 3.22A	0.1E	35	1. Change PR68 from 24.9K_1% to 21K_1% 2. Change PR65 from 14.3K_1% to 15.8K_1%	0.1	SST
9	Correct OCP of +VTT	Modify OCP current from 4.6A to 7A,because peak current of +VTT is 6A in spec.	0.1E	33	1. Change PR201 from 10K_1% to 14.3K_1% 2. Change PR209 from 15K_1% to 150K_1%	0.1	SST
10	Add ferrite bead for EMI	Based on EMI dept. test result, we must add bead and change capacity for EMI issue	0.1F	34	1. Add PL4 FBM-L11-453215-900LMAT 2. Change PC 24 from 0.1UF to 470PF and add PC23 470PF	0.3	PT
11	Add NI-MH battery	prevent NI-MH battery over charge/discharge	0.1F	34	Add PF1 7A fuse	0.3	PT
12	Plug in AC adapter and battery on time the system can't turn on.	Separate precharge path from VS net because leakage current is larger than p recharge current	0.1F	37	1. Connect pad2 of PD16 to VIN 2. Add PR20 1.5K and change PR84,PR85,and PR126 to 1.5K	0.3	PT
13	Safety protection for RTC battery	Add PR21 to prevent damging PR95 to damage RTC battery	0.1F	37	1.Add PR21 200 ohm	0.3	PT
14	Design margin is not enough	increase design margin for battery OVP prevent it misses	0.1F	35	Change battery OVP from 18.1V to 18.3V and BATT-OVP will be changed from 4V to 4.04V	0.3	PT

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15	noise issue from DC-DC	Change choice heigher capacitor	0.1F	35	Change PC60 form 2.2F_1206_25V to 4.7UF_1210_25	0.3	PT
16	Implement 6cell li-on	Add identifird signal 6C/8C#/4C#	0.1F	33	1.Add PR1 100K and PR2 1K_1% 2.Add PR3 no-pop	0.3	PT
17	modify charge voltage	Change 4S charge voltage to 17V for 4 cell/8 cell and NI-MH,other 3S is 12.75V for 6cell	0.1F	34	1. Change PR80 from 100K_0.1% to 152_0.1% 2. Change PR81 from 316K_0.1% to 309_0.1% 3. Add PR4 305K_0.1% and PR5 100K 4. Add PQ9 2N7002 and PQ10 DTC115EK 5. Add PC173 0.1U	0.3	PT
18	AC adapter is changed to 60W	modify constant power limited to 49W and disable air adapter	0.1G	33 34	1. No-pop PCN1 and Populate PCN3 2. No-pop PR29 and PQ11 3. Change PR68 from 21K_1% to 28.7K_1% 4. No-pop PQ30, PR65,PR131,PC101	0.3	PT
19	Add compensation solution for +5VALWP	The solution will reduce quantity of output capacitor and increase stability	0.1G	35	1. Populate PC122 47PF_0402 2. Populate PR179 2M_0402 3. Populate PR137 10.2K_0402_1% 4. Populate PC123 100PF_0402 5. Change PR136 from 0_0402 to 10K_0402_1%	0.3	PT
20	AC adapter is changed to 70W	modify constant power limited to 64W and support air line adaptor identified	0.1H	33 34	1. No-pop PCN3 and Populate PCN1 2. Populate PR29 and PQ11 3. Change PR68 from 28.7K_1% to 21K_1% 4. Populate PQ30, PR65,PR131,PC101	0.3	PT
21	Charger can't charge	Pin3 of PQ9 isn't connecttd pad2 of PR80	0.3C	34	Pin3 of PQ9 isn't connecttd pad2 of PR80	1.0	PT2
22	power limited for airline adapter is disabled	The control signal can't turn on PQ30	0.3C	34	1.Change control signal from AIR_ADP# to AIR_ADP 2.Change PQ30 from TP0610T to 2N7002	1.0	PT2
23	Delete on-pop component	Because the reverse component is not need	0.3C	35	Delete PC84,PC85,PC88	1.0	PT2
24	Add FUSE for safety of battery	Support NI-MH battery	0.3D	33	Reverse PF1 and add PJP4	1.0	ST
25	Fix Battery OVP protect point	Fix the table of Battery OVP and reserve PC115 about OP Amps oscillates	1.0	34	No-pop PC115	1.0	ST

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I tem	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
26	enhance conductivity of connector	enhance conductivity of battery connector based on customer's requirement	1.0	33	Change PCN2 from BTC-07GR1 to BTC-07GR4	1.0	ST
27	modify constant power limit spec.	modify constant power limited from 3.22A to 3.07A	1.0	34	1. Change PR68 from 21K_1% to 22.6_1% 2. Change PR65 from 15.8K_1% to 19.6K_1%	1.0	ST2
28	Fix DFX issue	The PL14 and PL15 is co-layout, but PL15 will not be used.	1.0	36	Delete PL15	1.0	ST2
29	Fix DFX issue	Delete PJP9 for SMT process.	1.0	36	Delete PJP9		

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